MBa335x
User's Manual

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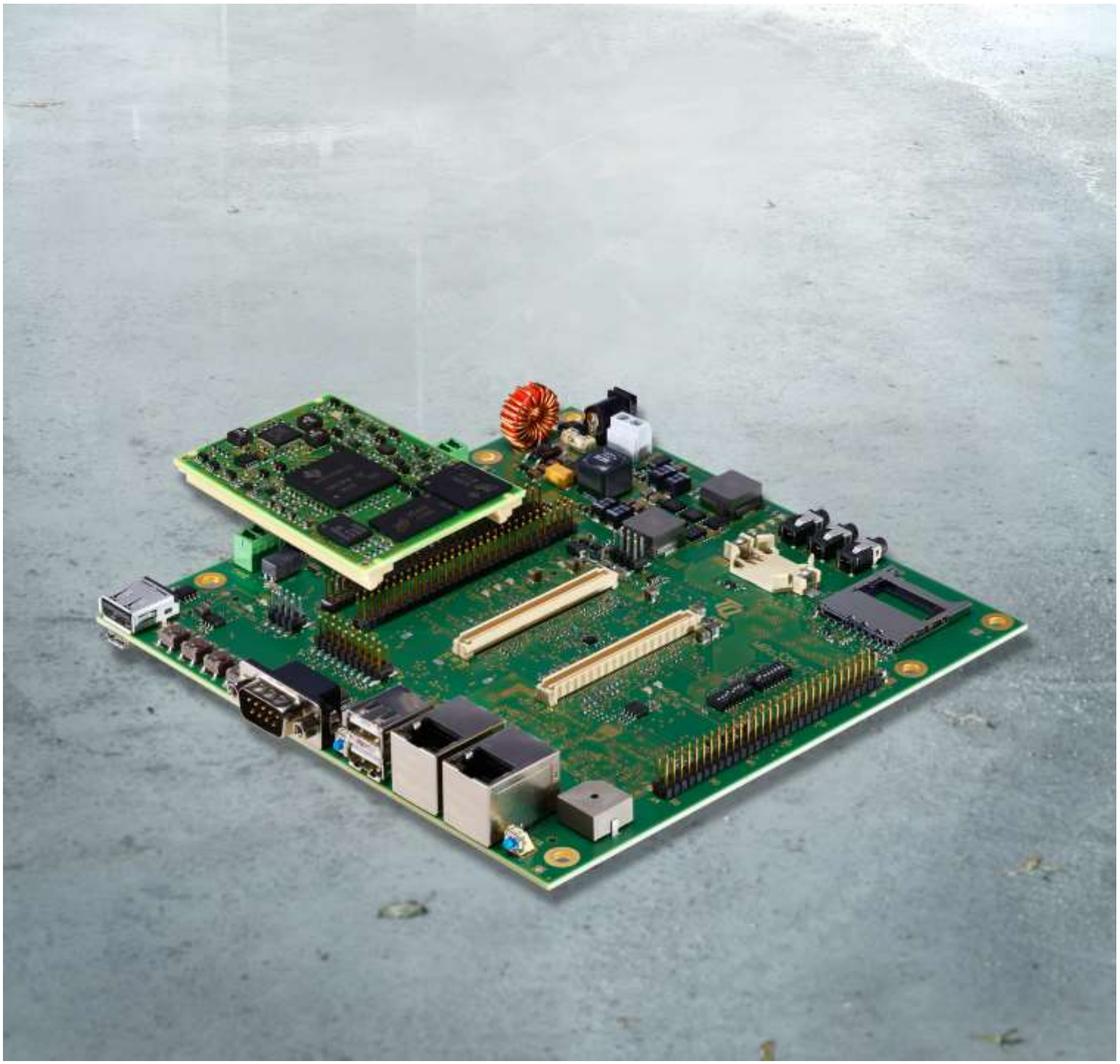

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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0200	05.10.2015	Petz		First issue

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa335x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- Circuit diagram MBa335x
- CPU Data Sheet Sitara AM335x
- User's Manual TQMa335x
- Documentation of boot loader U-Boot (http://www.denx.de/wiki/U-Boot/Documentation)
- Documentation of PTXdist (http://www.ptxdist.de)

2. BRIEF DESCRIPTION

The MBa335x is designed as a carrier board for the TQMa335x.

All of the TQMa335x interfaces are available on the MBa335x. The characteristics of the AM335x CPU can be evaluated, and therefore the software development for a TQMa335x project can be started immediately.

The MBa335x supports all TQMa335x modules with the TI CPUs AM3352, AM3354 and AM3359.

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 Block diagram

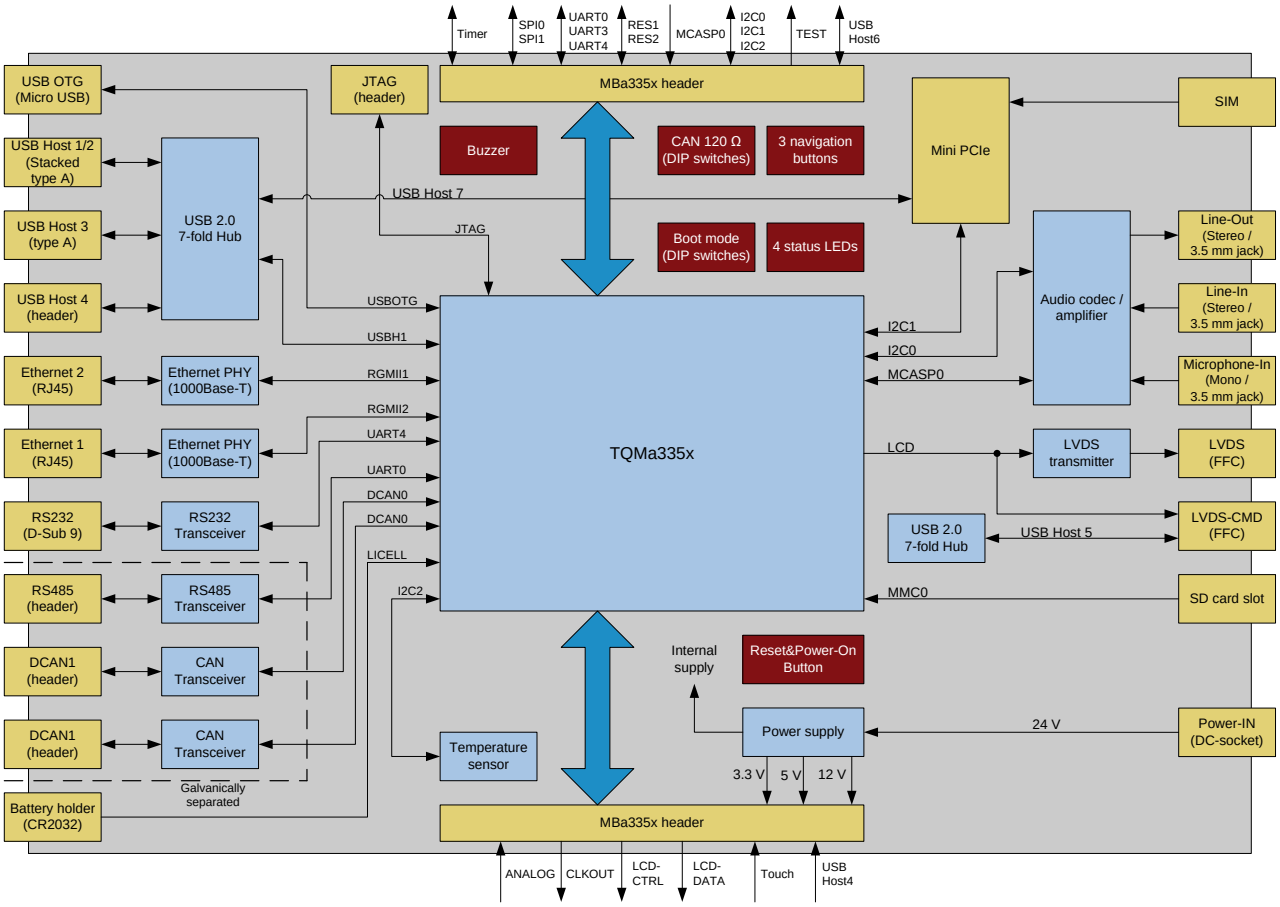


Illustration 1: Block diagram MBa335x

3.1.2 Functionality

The core of the system is the TQMa335x processor module with a Texas Instruments Sitara AM335x CPU.

The TQMa335x connects all peripheral components to each other.

In addition to the standard communication interfaces like USB, Ethernet, RS-232, RS-485, LVDS etc. all other available signals of the TQMa335x are routed to 2.54 mm standard headers.

The following interfaces / functions and user's interfaces are provided on the MBa335x:

Table 2: Overview interfaces

Interface	Qty.	Type of connector	Remark
USB 2.0 Hi-Speed host	2	USB receptacle type A	Dual port receptacle, right angle
USB 2.0 Hi-Speed host	1	USB receptacle type A	Single port receptacle, right angle
USB 2.0 Hi-Speed host	1	Header	
USB 2.0 Hi-Speed OTG	1	USB receptacle type Micro-AB	
Ethernet 1000BASE-T	1	RJ45 receptacle	Receptacle with integrated magnetics
CAN	2	Phoenix basic housing	Straight version, gal. separated
RS-485	1	Phoenix basic housing	Straight version, gal. separated
RS-232	1	D-Sub 9-pin connector	Right angle, Debug-UART
LVDS	1	DF19 receptacle	LVDS data
LVDS-CMD	1	DF19 receptacle	LVDS control lines
Audio Out	3	Jack 3.5 mm	1 × Line-out (stereo) 1 × Line-in (stereo) 1 × Microphone (mono)
SD card	1	Push-Pull type	
PCIe	1	Mini PCIe	
	1	SIM card holder	
JTAG	1	20-pin header, 2.54 mm pitch	
EMU	1	8-pin header, 2.54 mm pitch	
Headers	3	Header, 2.54 mm pitch	- USB Host 6, Host 4 - Test - I2C0, I2C1, I2C2 - MCASP0 - RES1, RES2 - UART0, UART3, UART4 - SPI0, SPI1 - Timer - Touch - LCD-CTRL, LCD-DATA - CLKOUT - ANALOG
Power In	1	DC jack (2.5 mm / 5.5 mm)	
(V_{IN} = 24 V ±5 % DC)	1	DC jack 2-pin (screw terminals)	
Power Out header	1	Header, 2.54 mm pitch	- 3.3 V @ 2 A - 5 V @ 2 A - 12 V @ 3 A
Backup supply	1	8-pin header, 2.54 mm pitch	
Battery holder	1	CR2032 holder	Backup battery RTC

Table 3: Overview diagnose and user's interfaces

Interface	Qty.	Component	Remark
Status-LEDs	18	Chip LEDs	Among others Power-LEDs, LEDs at GPIOs, …
Temperature sensor	1		
Power / reset button	3	Push button	
Navigation buttons	3	Push button	
Boot-Mode configuration	16	DIP switch	
CAN - and RS-485 termination	4	DIP switch	
Signal generator	1	Buzzer	

4. ELECTRONICS

4.1 System components

4.1.1 TQMa335x

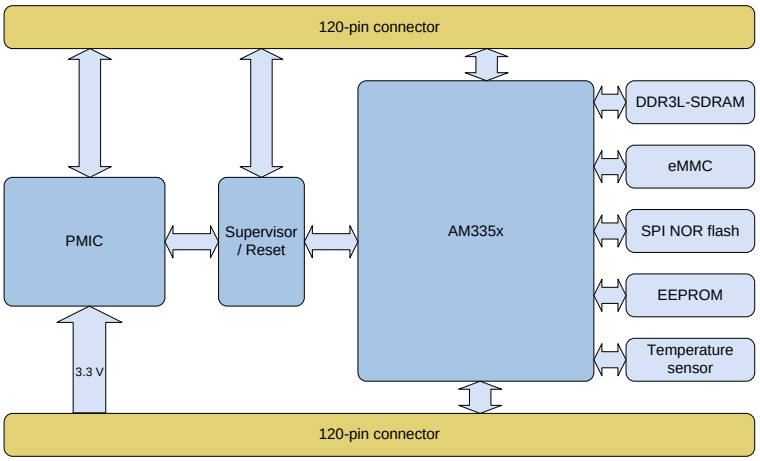


Illustration 2: Block diagram TQMa335x

The TQMa335x with the AM335x CPU is the central system component. It provides DDR3L-SDRAM, eMMC, NOR flash and EEPROM memory. All voltages required by the TQMa335x are derived from the supply voltage of 3.3 V.

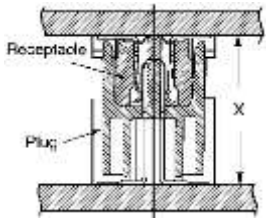
The available signals are routed to two connectors on the MBa335x. More detailed information is to be taken from the accompanying User's Manual of the TQMa335x.

The boot behaviour of the TQMa335x can be customised. The required boot-mode configuration can be set with DIP switches, see section 4.3.5.

The connector used on the MBa335x is shown in Table 4.

If a different board-to-board distance is required, higher connectors can be used. Suitable types are to be taken from Table 4.

Table 4: Suitable carrier board mating connectors

Manufacturer	Pin count / Part number	Remark	Stack height (X)	
TE connectivity	120-pin: 5177986-5	Used on MBa335x	5 mm	
TE connectivity	120-pin: 1-5177986-5	Alternative	6 mm	
TE connectivity	120-pin: 2-5177986-5	Alternative	7 mm	
TE connectivity	120-pin: 3-5177986-5	Alternative	8 mm	

The pins assignment listed in Table 5 and Table 6 refer to the corresponding standard BSP of TQ-Systems GmbH.
Information regarding I/O in Table 5 and Table 6 refer to the CPU pins.

Attention:	
	Depending on the selected TQMa335x, not all interfaces are available. Available interfaces are to be taken from the User's Manual and the pinout table of the TQMa335x.

Table 5: Pinout connector X1

Ball	I/O	Level	Group	Signal	Pin		Pin	Signal	Group	Level	I/O	Ball
–	P	0 V	Power	DGND	1		2	DGND	Power	0 V	P	–
–	I	3.3 V	CONFIG	PMIC_SLEEP	3		4	PMIC_PWRON	CONFIG	3.3 V	I	–
–	O	3.3 V	CONFIG	RTC_INT#	5		6	PMIC_INT	CONFIG	3.3 V	O	–
U18	I/O	3.3 V	GPIO	GPIO1_28	7		8	TEMP_OS#	CONFIG	3.3 V	O	–
V6	I/O	3.3 V	GPIO	GPIO1_29	9		10	PWRONRST_IN#	CONFIG	3.3 V	I	–
T13	I/O	3.3 V	GPIO	GPIO2_0	11		12	PWRONRST_OUT#	CONFIG	3.3 V	O	–
C5	I	1.8 V	CONFIG	EXT_WAKEUP	13		14	EXTINT#	CONFIG	3.3 V	O	B18
–	P	0 V	Power	DGND	15		16	DGND	Power	0 V	P	–
R17	A	3.3 V	USB	USB_OTG.D_P	17		18	USB_H.D_P	USB	3.3 V	A	N17
R18	A	3.3 V	USB	USB_OTG.D_N	19		20	USB_H.D_N	USB	3.3 V	A	N18
–	P	0 V	Power	DGND	21		22	DGND	Power	0 V	P	–
P18	A	3.3 V	USB	USB1_CE	23		24	USB0_CE	USB	3.3 V	A	M15
P17	A	3.3 V	USB	USB_OTG.ID	25		26	USB0_ID	USB	3.3 V	A	P16
T18	A	3.3 V	USB	USB1_VBUS	27		28	USB0_VBUS	USB	3.3 V	A	P15
F15	O	3.3 V	USB	USB_OTG.PWR_EN	29		30	USB0_DRVBUS	USB	3.3 V	O	F16
–	P	0 V	Power	DGND	31		32	DGND	Power	0 V	P	–
C15	I	3.3 V	UART	UART3.RX	33		34	UART3.TX	UART	3.3 V	O	C18
G16	I/O	3.3 V	MMC	MMC0.DAT0	35		36	MMC0.DAT2	MMC	3.3 V	I/O	F18
G15	I/O	3.3 V	MMC	MMC0.DAT1	37		38	MMX0.DAT3	MMC	3.3 V	I/O	F17
–	P	0 V	Power	DGND	39		40	DGND	Power	0 V	P	–
G17	I/O	3.3 V	MMC	MMC0.CLK	41		42	MMC0.CMD	MMC	3.3 V	I/O	G18
–	P	0 V	Power	DGND	43		44	DGND	Power	0 V	P	–
H17	I/O	3.3 V	SPI	SPI1.MOSI	45		46	SPI1.MISO	SPI	3.3 V	I/O	J15
H16	I/O	3.3 V	SPI	SPI1.SCLK	47		48	SPI1.CS0	SPI	3.3 V	I/O	H18
–	P	0 V	Power	DGND	49		50	DGND	Power	0 V	P	–
D18	O	3.3 V	CAN	DCAN0_TX	51		52	DCAN1_TX	CAN	3.3 V	O	E18
D17	I	3.3 V	CAN	DCAN0_RX	53		54	DCAN1_RX	CAN	3.3 V	I	E17
–	P	0 V	Power	DGND	55		56	DGND	Power	0 V	P	–
D14	O	3.3 V	DIV	CLKOUT.2	57		58	CLKOUT.1	DIV	3.3 V	O	A15
–	P	0 V	Power	DGND	59		60	DGND	Power	0 V	P	–
D12	I/O	3.3 V	Audio	MCASP0.AXR0	61		62	MCASP0_FSR	Audio	3.3 V	I/O	C13
D13	I/O	3.3 V	Audio	MCASP0_AXR1	63		64	MCASP0.FSX	Audio	3.3 V	I/O	B13
C12	I/O	3.3 V	Audio	MCASP0.AXR2	65		66	MCASP0.ACLKR	Audio	3.3 V	I/O	B12
A14	I/O	3.3 V	Audio	MCASP0_AXR3	67		68	MCASP0.ACLKX	Audio	3.3 V	I/O	A13
–	P	0 V	Power	DGND	69		70	DGND	Power	0 V	P	–
C9	A	1.8 V	ADC	ANALOG.AIN7	71		72	ANALOG.AIN3	ADC	1.8 V	A	A7
A8	A	1.8 V	ADC	ANALOG.AIN6	73		74	ANALOG.AIN2	ADC	1.8 V	A	B7
–	P	0 V	Power	DGND	75		76	DGND	Power	0 V	P	–
B8	A	1.8 V	ADC	ANALOG.AIN5	77		78	ANALOG.AIN1	ADC	1.8 V	A	C7
C8	A	1.8 V	ADC	ANALOG.AIN4	79		80	ANALOG.AIN0	ADC	1.8 V	A	B6
–	P	0 V	Power	DGND	81		82	DGND	Power	0 V	P	–
B17	I/O	3.3 V	SPI	SPI0.MISO	83		84	SPI0.MOSI	SPI	3.3 V	I/O	B16
A17	I/O	3.3 V	SPI	SPI0.SCLK	85		86	SPI0.CS0	SPI	3.3 V	I/O	A16
–	P	0 V	Power	DGND	87		88	DGND	Power	0 V	P	–
–	–	–	N.C.	RES1.SPARE1	89		90	RES1.SPARE2	N.C.	–	–	–
D16	I/O	3.3 V	I2C	I2C1.SDA	91		92	I2C1.SCL	I2C	3.3 V	I/O	D15
E15	I	3.3 V	UART	UART0.RX	93		94	UART0.TX	UART	3.3 V	O	E16
–	P	0 V	Power	DGND	95		96	DGND	Power	0 V	P	–
A10	I/O	3.3 V	CONFIG	WARMRST#	97		98	JTAG.TRST#	JTAG	3.3 V	I	B10
A11	O	3.3 V	JTAG	JTAG.TD0	99		100	JTAG.EMU1	JTAG	3.3 V	I/O	B14
B11	I	3.3 V	JTAG	JTAG.TDI	101		102	JTAG.EMU0	JTAG	3.3 V	I/O	C14
C11	I	3.3 V	JTAG	JTAG.TMS	103		104	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	105		106	JTAG.TCK	JTAG	3.3 V	I	A12
–	P	1.5 V	CONFIG	TEST.VDDS-DDR	107		108	DGND	Power	0 V	P	–
–	P	1.8 V	CONFIG	TEST.VDDS	109		110	RES1.SPARE3	N.C.	–	–	–
–	P	1.8 V	CONFIG	TEST.VDD-PLL	111		112	RES1.SPARE4	N.C.	–	–	–
–	P	1.8 V	CONFIG	TEST.VDD-USB	113		114	TEST.VDD-CORE	CONFIG	1.1 V	P	–
–	P	1.8 V	CONFIG	TEST.VDDA-ADC	115		116	TEST.VDDS-MPU	CONFIG	1.1 V	P	–
–	P	1.8 V	CONFIG	TEST.VDDS-RTC	117		118	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	119		120	DGND	Power	0 V	P	–

Table 6: Pinout connector X2

Ball	I/O	Level	Group	Signal	Pin		Pin	Signal	Group	Level	I/O	Ball
–	P	3.3 V	Power	VCC3V3_TQMA335X	1		2	VCC3V3_TQMA335X	Power	3.3 V	P	–
–	P	3.3 V	Power	VCC3V3_TQMA335X	3		4	VCC3V3_TQMA335X	Power	3.3 V	P	–
–	P	3.3 V	Power	VCC3V3_TQMA335X	5		6	VCC3V3_TQMA335X	Power	3.3 V	P	–
–	P	0 V	Power	DGND	7		8	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	9		10	DGND	Power	0 V	P	–
–	P	0 V	Power	DGND	11		12	DGND	Power	0 V	P	–
–	P	3.3 V	Power	VBACKUP_RTC	13		14	VBACKUP_PMIC	Power	3.3 V	P	–
–	P	0 V	Power	DGND	15		16	DGND	Power	0 V	P	–
C17	I/O	3.3 V	I2C	I2C0.SDA	17		18	VDDSH3V3	Power	3.3 V	P	–
C16	I/O	3.3 V	I2C	I2C0.SCL	19		20	RES2.SPARE1	N.C.	–	–	–
–	P	0 V	Power	DGND	21		22	DGND	Power	0 V	P	–
K18	I	3.3 V	RGMII	RGMII_1.TCLK	23		24	RGMII_1.RCLK	RGMII	3.3 V	I	L18
–	P	0 V	Power	DGND	25		26	DGND	Power	0 V	P	–
J16	O	3.3 V	RGMII	RGMII_1.TCTL	27		28	RGMII_1.RCTL	RGMII	3.3 V	I	J17
K17	O	3.3 V	RGMII	RGMII_1.TD0	29		30	RGMII_1.RD0	RGMII	3.3 V	I	M16
K16	O	3.3 V	RGMII	RGMII_1.TD1	31		32	RGMII_1.RD1	RGMII	3.3 V	I	L15
K15	O	3.3 V	RGMII	RGMII_1.TD2	33		34	RGMII_1.RD2	RGMII	3.3 V	I	L16
J18	O	3.3 V	RGMII	RGMII_1.TD3	35		36	RGMII_1.RD3	RGMII	3.3 V	I	L17
–	P	0 V	Power	DGND	37		38	DGND	Power	0 V	P	–
M18	O	3.3 V	MII	ENET_MDC	39		40	ENET_MDIO	MII	3.3 V	I/O	M17
T17	I	3.3 V	UART	UART4.RX	41		42	UART4.TX	UART	3.3 V	O	U17
–	P	0 V	Power	DGND	43		44	DGND	Power	0 V	P	–
U15	O	3.3 V	RGMII	RGMII_2.TCLK	45		46	RGMII_2.RCLK	RGMII	3.3 V	I	T15
–	P	0 V	Power	DGND	47		48	DGND	Power	0 V	P	–
R13	O	3.3 V	RGMII	RGMII_2.TCTL	49		50	RGMII_2.RCTL	RGMII	3.3 V	I	V14
V15	O	3.3 V	RGMII	RGMII_2.TD0	51		52	RGMII_2.RD0	RGMII	3.3 V	I	V17
R14	O	3.3 V	RGMII	RGMII_2.TD1	53		54	RGMII_2.RD1	RGMII	3.3 V	I	T16
T14	O	3.3 V	RGMII	RGMII_2.TD2	55		56	RGMII_2.RD2	RGMII	3.3 V	I	U16
U14	O	3.3 V	RGMII	RGMII_2.TD3	57		58	RGMII_2.RD3	RGMII	3.3 V	I	V16
–	P	0 V	Power	DGND	59		60	DGND	Power	0 V	P	–
U7	I/O	3.3 V	MMC	MMC1.DAT0	61		62	MMC1.DAT4	MMC	3.3 V	I/O	U8
V7	I/O	3.3 V	MMC	MMC1.DAT1	63		64	MMC1.DAT5	MMC	3.3 V	I/O	V8
R8	I/O	3.3 V	MMC	MMC1.DAT2	65		66	MMC1.DAT6	MMC	3.3 V	I/O	R9
T8	I/O	3.3 V	MMC	MMC1.DAT3	67		68	MMC1.DAT7	MMC	3.3 V	I/O	T9
–	P	0 V	Power	DGND	69		70	DGND	Power	0 V	P	–
V9	I/O	3.3 V	MMC	MMC1.CMD	71		72	MMC1.CLK	MMC	3.3 V	I/O	U9
–	P	0 V	Power	DGND	73		74	DGND	Power	0 V	P	–
V12	O	3.3 V	LCD	LCD_MCLK	75		76	LCD_HSYNC	LCD	3.3 V	O	R5
–	P	0 V	Power	DGND	77		78	DGND	Power	0 V	P	–
V5	O	3.3 V	LCD	LCD_PCLK	79		80	LCD_AC_BIAS_EN#	LCD	3.3 V	O	R6
–	P	0 V	Power	DGND	81		82	DGND	Power	0 V	P	–
U10	O	3.3 V	LCD	LCD_DAT23	83		84	LCD_DAT22	LCD	3.3 V	O	T10
T11	O	3.3 V	LCD	LCD_DAT21	85		86	LCD_DAT20	LCD	3.3 V	O	U12
T12	O	3.3 V	LCD	LCD_DAT19	87		88	LCD_DAT18	LCD	3.3 V	O	R12
V13	O	3.3 V	LCD	LCD_DAT17	89		90	LCD_DAT16	LCD	3.3 V	O	U13
–	P	0 V	Power	DGND	91		92	DGND	Power	0 V	P	–
T5	I/O	3.3 V	LCD/ BOOT	LCD_DAT15	93		94	LCD_DAT14	LCD/ BOOT	3.3 V	I/O	V4
V3	I/O	3.3 V	LCD/ BOOT	LCD_DAT13	95		96	LCD_DAT12	LCD/ BOOT	3.3 V	I/O	V2
U4	I/O	3.3 V	LCD/ BOOT	LCD_DAT11	97		98	LCD_DAT10	LCD/ BOOT	3.3 V	I/O	U3
U2	I/O	3.3 V	LCD/ BOOT	LCD_DAT9	99		100	LCD_DAT8	LCD/ BOOT	3.3 V	I/O	U1
–	P	0 V	Power	DGND	101		102	DGND	Power	0 V	P	–
T4	I/O	3.3 V	LCD/ BOOT	LCD_DAT7	103		104	LCD_DAT6	LCD/ BOOT	3.3 V	I/O	T3
T2	I/O	3.3 V	LCD/ BOOT	LCD_DAT5	105		106	LCD_DAT4	LCD/ BOOT	3.3 V	I/O	T1
R4	I/O	3.3 V	LCD/ BOOT	LCD_DAT3	107		108	LCD_DAT2	LCD/ BOOT	3.3 V	I/O	R3
R2	I/O	3.3 V	LCD/ BOOT	LCD_DAT1	109		110	LCD_DAT0	LCD/ BOOT	3.3 V	I/O	R1
–	P	0 V	Power	DGND	111		112	DGND	Power	0 V	P	–
–	–	–	N.C.	RES2.SPARE2	113		114	RES2.SPARE3	N.C.	–	–	–
R7	I/O	3.3 V	DIV	TIMER.4	115		116	TIMER.6	DIV	3.3 V	I/O	U6
T6	I/O	3.3 V	DIV	TIMER.5	117		118	TIMER.7	DIV	3.3 V	I/O	T7
–	P	0 V	Power	DGND	119		120	DGND	Power	0 V	P	–

4.1.2 I²C address mapping

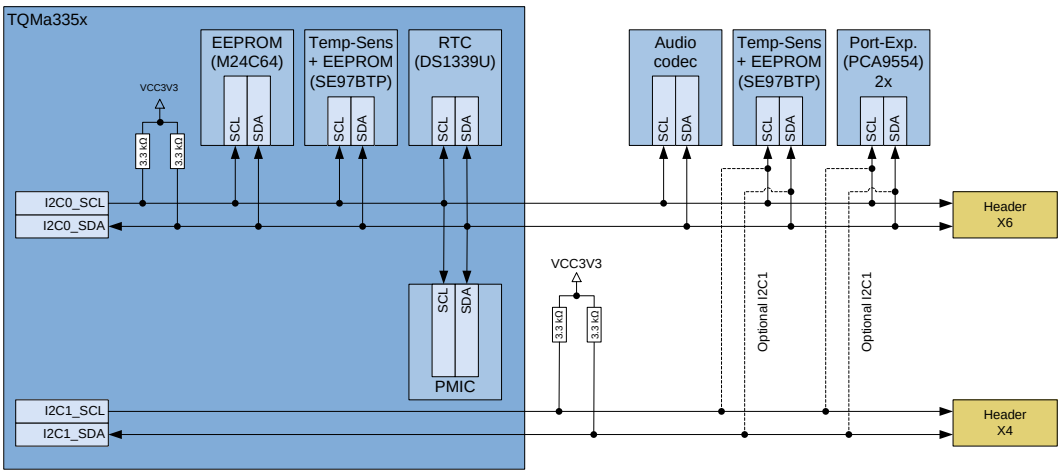


Illustration 3: Block diagram I2C bus

Only I2C0 is used on the MBa335x by default. I2C1 is used neither on the MBa335x nor on the TQMa335x by default.
I2C0 and I2C1 are routed to headers on the MBa335x.
Table 7 shows the slave addresses used for this bus as well as the components on the TQMa335x.
The temperature sensor/EEPROM, as well as both port expanders can be controlled with I2C1 by an assembly option on the MBa335x. See Table 8 for the required assembly option to use the I2C1 bus.

Table 7: I2C0 slave address mapping (default assembly)

				Address						
	Component	Ref.	Hex	MSB		Binary				LSB
TQMa335x	EEPROM (M24C64)	–	0x50	1	0	1	0	0	0	0
	EEPROM (SE97BTP)	–	0x57	1	0	1	0	1	1	1
	Temperature sensor (SE97BTP)	–	0x1F	0	0	1	1	1	1	1
	RTC (DS1339U)	–	0x68	1	1	0	1	0	0	0
	PMIC (TPS659)	–	0x2D	0	1	0	1	1	0	1
	PMIC (TPS659)	–	0x12	0	0	1	0	0	1	0
MBa335x	Audio codec (TLV320)	N2200	0x18	0	0	1	1	0	0	0
	EEPROM (SE97BTP)	D2400	0x51	1	0	1	0	0	0	1
	Temperature sensor (SE97BTP)	D2400	0x19	0	0	1	0	0	0	1
	Port expander (PCA9554) outputs	D900	0x20	0	1	0	0	0	0	0
	Port expander (PCA9554) inputs	D901	0x21	0	1	0	0	0	0	1

Table 8: Assembly option for port expander and temperature sensor

Option	R900	R901	R902	R903	R2400	R2405	R2406	R2411
Port-Expander at I2C0 (Default assembly)	0 Ω	NP	0 Ω	NP	X			
Port-Expander at I2C1	NP	0 Ω	NP	0 Ω				
Temperature sensor at I2C0 (Default assembly)	X				0 Ω	NP	0 Ω	NP
Temperature sensor at I2C1					NP	0 Ω	NP	0 Ω

Attention:

Attention when using I2C0. Since the PMIC can be addressed via this interface, errors on the bus can lead to instabilities of the TQMa335x!

4.1.3 Temperature sensor

SE97BTP temperature sensors with integrated EEPROM are available on the TQMa335x and the MBa335x to monitor temperatures. Both sensors are connected to I2C0 or I2C1. Each of them has an individual device address (see 4.1.2 for address mapping).

Table 9: Electrical characteristics SE97BTP

Parameter	Value	Range
Accuracy	±2 °C ±3 °C	+40 °C to +125 °C –40 °C to +125 °C
Resolution	0.125 °C	11 bit

The SE97BTP on the top side of the MBa335x is located between the connectors for the TQMa335x, the SE97BTP on the TQMa335x is on the bottom side of the module.

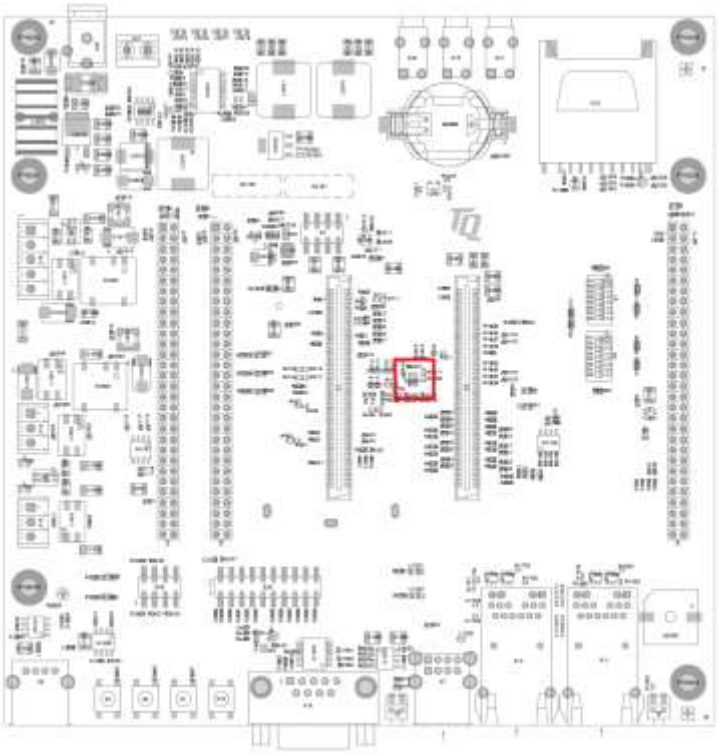


Illustration 4: Position of temperature sensor SE97BTP (D2400) on MBa335x

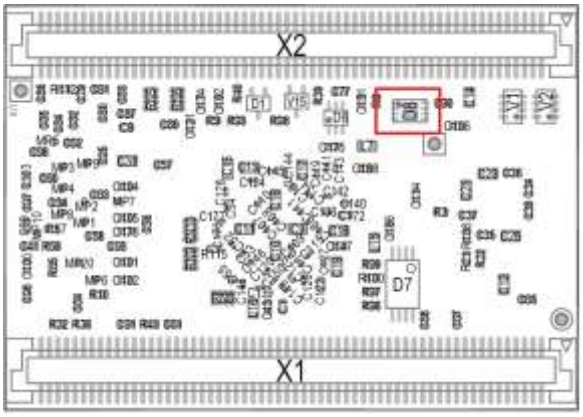


Illustration 5: Position of temperature sensor SE97BTP (D8) on TQMa335x

4.1.4 RTC backup supply

The MBa335x does not provide an RTC. On the TQMa335x the following RTCs are available, which are supplied by the MBa335x in case of a backup:

- RTC in the CPU AM335x
- RTC in the PMIC TPS65910
- RTC DS1339U (optional)

A coin cell on the MBa335x supplies the RTC on the TQMa335x. With jumper X3 the coin cell either supplies the PMIC and with it the CPU-internal RTC, or the optional RTC DS1339U.
Technical information about the power modes of the PMIC, as well as the CPU, is provided in the data sheets (see [1] and [2]).

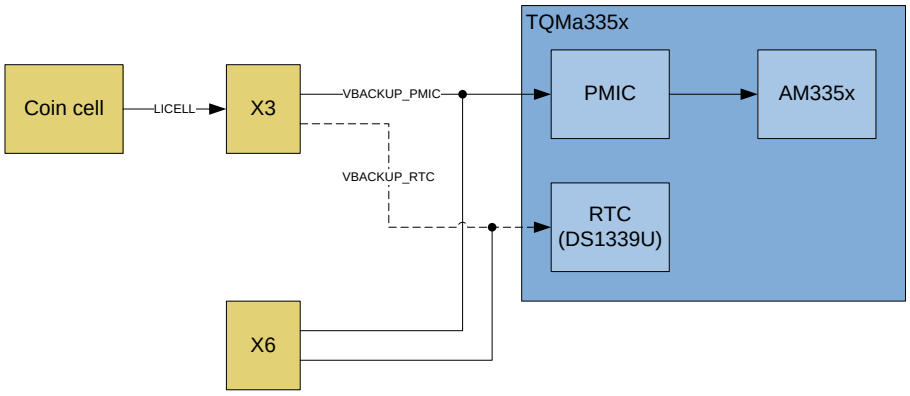


Illustration 6: RTCs supplies on TQMa335x

The following table shows the electrical characteristics of the RTCs.

Table 10: Electrical characteristics of RTCs

RTC	Parameter	Min.	Typ.	Max.	Unit
PMIC / AM335x	Backup voltage VBACKUP_PMIC	2.2[1]	–	3.0	V
	Current consumption	–	25	–	µA
DS1339U	Backup voltage VBACKUP_RTC	1.3	3.0	3.7	V
	Current consumption	–	0.4	1.0	µA

The RTC on the MBa335x is on the bottom side, near the audio codec.
The header for the battery supply is on the top side, next to the SD card holder.

Table 11: RTC backup supply

Manufacturer / Number	Description	Package
Sony / CR2032	Lithium battery 3.0 V, 220 mAh	MECH
RENATA / SMTU2032	CR2032 battery holder	SMD2

1: Threshold VBNPR of TPS65910.

4.1.5 Power and Reset

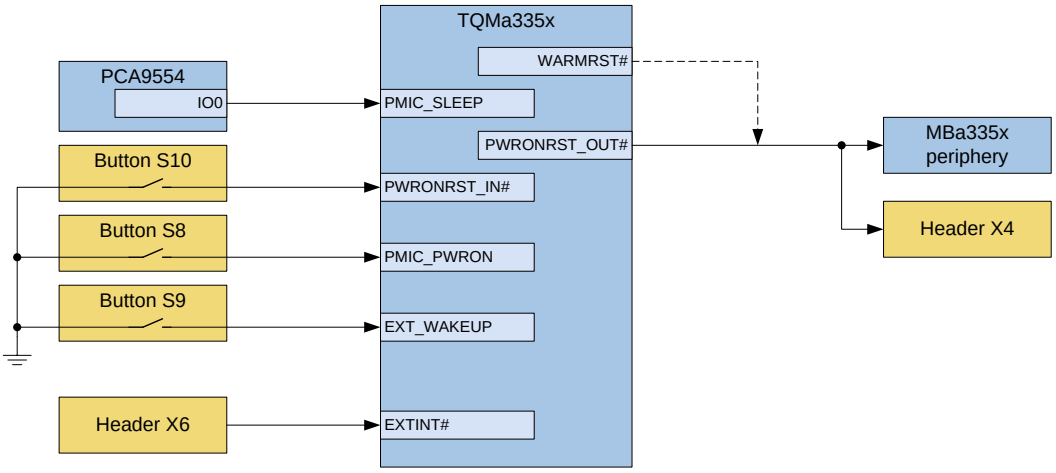


Illustration 7: Block diagram Power and Reset

The MBa335x provides several options to trigger a complete or partial reset of the TQMa335x.
Two reset sources are available to reset sections of the circuitry on the MBa335x.

- **WARMRST#**: Reset output of the AM335x; Low-active
- **PWRONRST_OUT#**: Reset output of the PMIC; Low-active; default assembly

Depending on the assembly option (see Table 12) both signals can be used as STKRST# signal to reset the following components on the MBa335x:

- USB 2.0 Hi-Speed Hub USB2517 (D1600)
- Ethernet 1 Phy KSZ9031 (D1400)
- Ethernet 2 Phy KSZ9031 (D1600)
- Reset output at LVDS-CMD (X18)
- Audio-Codec TLV320A (N2200)
- Mini PCIe (X22)

For external components PWRONRST_OUT is routed to connector X4.

Table 12: Option of reset source for MBa335x-Reset

Option	R427	R428
STKRST# at WARMRST#	0 Ω	NP
STKRST# at PWRONRST_OUT# (Default)	NP	0 Ω

The signal PMIC_SLEEP can be set with port expander D900. A falling edge triggers the Sleep Mode of the PMIC (see [2]). With the three buttons S8, S9 and S10 on the MBa335x different power modes can be entered or left.

- S8 (PWRON): PMIC starts from OFF/SLEEP state; internal debouncing
- S9 (EXT_WAKEUP): External Wake event of the AM335x
- S10 (PWRONRST_IN#): CPU-Reset; generates Reset on MBa335x via STKRST#

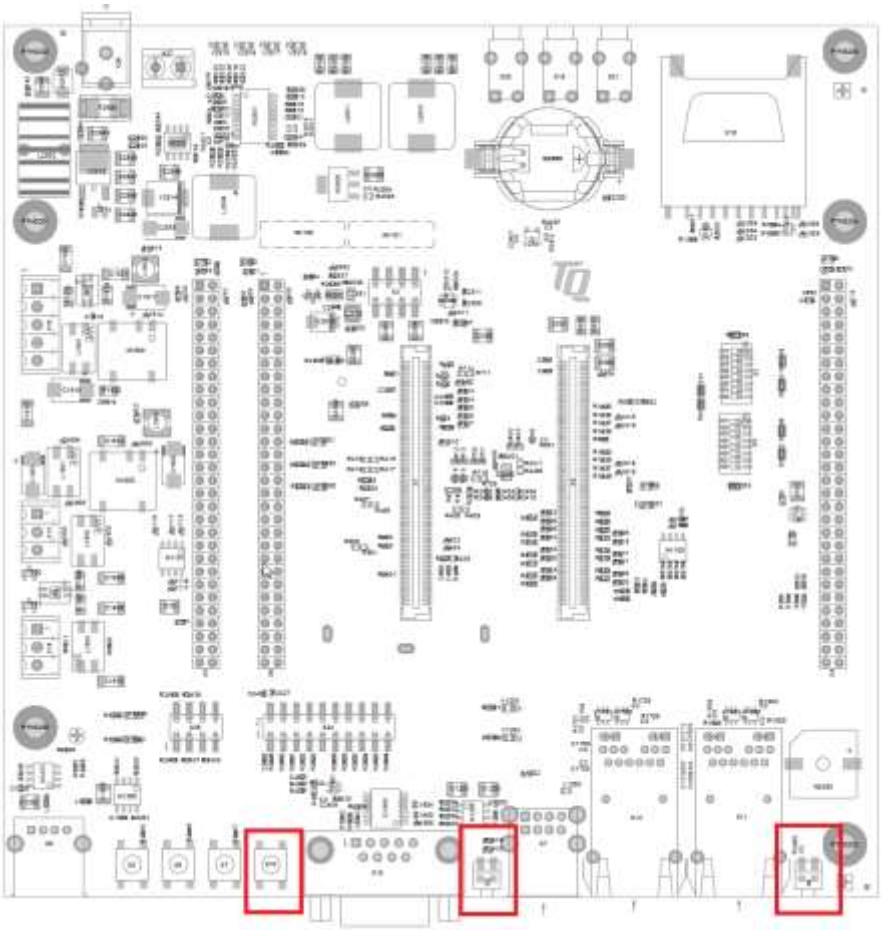


Illustration 8: Position push buttons S8, S9, S10

Table 13: Reset/Power buttons

Manufacturer / Number	Description	Package
Knitter Switch / TSS 61N	Push button	SMT4
Knitter Switch / TMSE 10J-RA	Push button	SMT4

4.1.6 Port-Expander

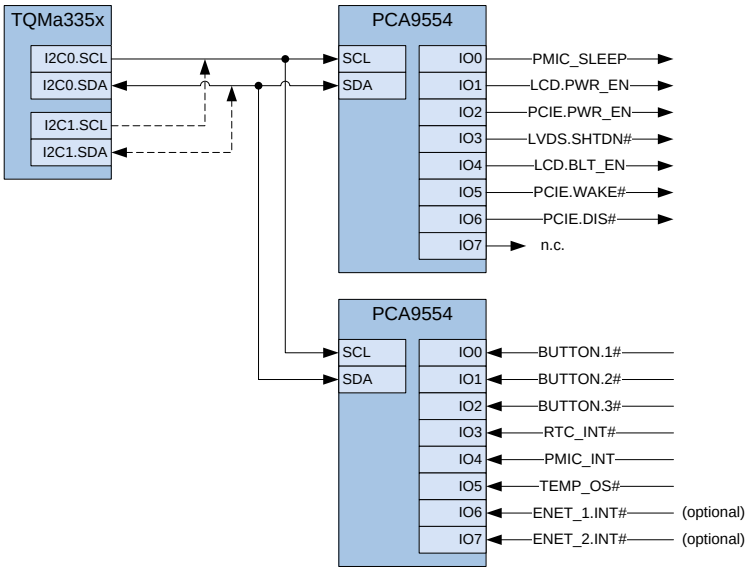


Illustration 9: Block diagram Port-Expander

The MBa335x provides two port expanders. D900 only provides outputs, D901 only provides inputs.

Attention:	
	Depending on their primary function the port expanders should either be configured as inputs or outputs to avoid functionality interference.

The port expanders are controlled by I2C0 by default as shown in section 4.1.2. I2C1 can be used with an assembly option. The following table shows the signals used at the port expander.

Table 14: Signals at Port-Expander

Device	Port	I/O	Signal	Target / Source
D900	IO0	Output	PMIC_SLEEP	→ PMIC Pin SLEEP on TQMa335x
	IO1		LCD.PWR_EN	→ LVDS-CMD connector X18, → header X4 on MBa335x, optional PU/PD to VCC3V3
	IO2		PCIE.PWR_EN	→ Pin ON/OFF of VCC3V3_MPCIE regulator N2300, 10 kΩ PD to GND, optional PU to VCC3V3
	IO3		LVDS.SHTDN#	→ Pin SHTDN# of LVDS-Transmitter D2000, 10 kΩ PD to GND, optional PU to VCC3V3
	IO4		LCD.BLT_EN	→ LVDS-COMD connector X18, → header X4 on MBa335x, 10 kΩ PD to GND, optional PU to VCC3V3
	IO5		PCIE.WAKE#	→ Mini PCIe connector X22, 10 kΩ PU to VCC3V3, optional PD to GND
	IO6		PCIE.DIS#	→ Mini PCIe connector X22, 10 kΩ PD to GND, optional PU to VCC3V3
	IO7		n.c.	
D901	IO0	Input	BUTTON.1#	→ Navigation button S5, 10 kΩ PU to VCC3V3
	IO1		BUTTON.2#	→ Navigation button S6, 10 kΩ PU to VCC3V3
	IO2		BUTTON.3#	→ Navigation button S7, 10 kΩ PU to VCC3V3
	IO3		RTC_INT#	→ Pin SQW/INT# of RTC DS1339 on TQMa335x, 10 kΩ PU to VCC3V3
	IO4		PMIC_INT	→ PMIC Pin IN1 on TQMa335x, → MBa335x header X6
	IO5		TEMP_OS#	→ Pin EVENT# of EEPROM SE97BTP on TQMa335x, 10 kΩ PU to VCC3V3, → header X6 on MBa335x
	IO6		n.c.	optional at ENET_1.INT#, see Table 32
	IO7		n.c.	optional at ENET_2.INT#, see Table 32

4.1.7 Further configuration options

The MBa335x provides additional options to configure the available module pins. This applies to several interfaces, and is implemented partially by multistage assembly options.

Table 15 to Table 17 show the assembly options sorted by module signal name, if the module signal names are not already described in other sections.

4.1.8 Real-Time Unit (PRU)

The real time Unit of the AM335x was not tested, but can however be used at header X4. See data sheet of the AM335x for appropriate multiplexing. More signals must be multiplexed to header X4 for full functionality:

Table 15: Placement option PR1_UART0_CTS#

Option	R412	R413	R707	R708	Remark
DCAN0_TX an DCAN0.TX ANALOG.AIN2 an Touch_Y+	0 Ω	NP	0 Ω	NP	Default
DCAN0_TX an Touch_Y+	NP	0 Ω	NP	0 Ω	For usage of PR1_UART0_CTS# at X4

Table 16: Placement option PR1_UART0_RTS#

Option	R414	R415	R709	R710	Remark
DCAN0_RX an DCAN0.RX ANALOG.AIN0 an Touch_X+	0 Ω	NP	0 Ω	NP	Default
DCAN0_RX an Touch_X+	NP	0 Ω	NP	0 Ω	For usage of PR1_UART0_RTS# at X4

Table 17: Placement option PR1_MDIO_DATA

Option	R420	R421	R711	R712	Remark
GPIO2_0 an GPIO2.0 ANALOG.AIN3 an Touch_Y–	0 Ω	NP	0 Ω	NP	Default
GPIO2_0 an Touch_Y–	NP	0 Ω	NP	0 Ω	For usage of PR1_MDIO_DATA at X4

4.1.9 Power supply

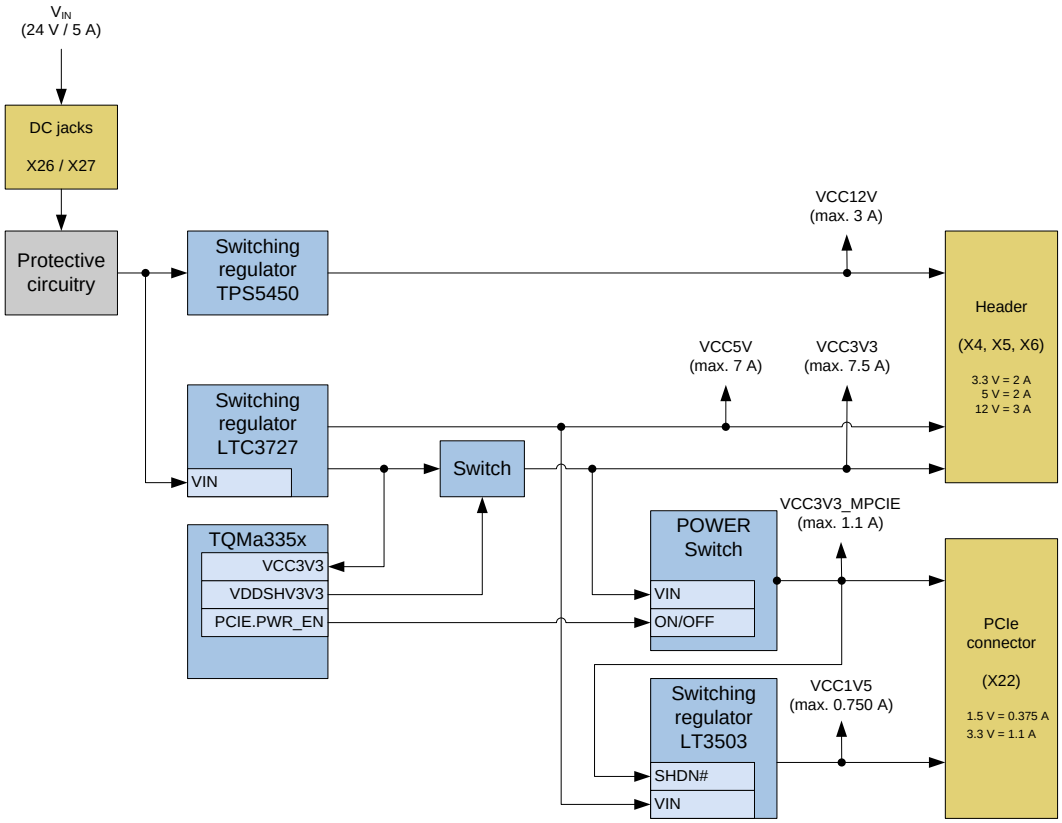


Illustration 10: Block diagram power supply

The MBa335x is supplied with 24 V via X26 or X27. From this voltage 1.5 V, 3.3 V, 5 V and 12 V are generated on the MBa335x. These voltages are used to supply the components on the MBa335x.

Additionally, 3.3 V, 5 V and 12 V are available at each of the three headers X4, X5 and X6 on the MBa335x.
All three connectors share the available power (3.3 V / 2 A, 5 V / 2 A, 12 V / 3 A).

1.5 V is only available at the PCIe connector X22. The 1.5 V rail can supply a maximum of 0.375 A.

The supply of the MBa335x is only switched on by 3.3 V when the power supply of the TQMa335x is up completely to avoid cross supply by the MBa335x. Hence, the circuitry with the Power-FET as a switch for VCC3V3 should also be used in customer designs.

Attention:	
	In the own design, the VCC3V3 should be switched on or off with the signal VDDSHV3V3 from the TQMa335x, to avoid cross supply and errors in the power-up/down sequence.

On the MBa335x the input voltage of 24 V has the following protective circuitry (see also Illustration 10):

- Fuse
- Excess voltage protection diode
- PI filter
- Inverse-polarity protection
- Capacitors for voltage smoothing

Table 18: Parameter of protective circuit

Parameter	Min.	Typ.	Max.	Unit
Overcurrent limitation by fuse (inertly)	–	5	–	A
Excess voltage limitation by SMBJ24CA	26.7	–	26.9	V

Under full load the assembly has a maximum power consumption of 94 W (all supply voltages are loaded with maximum current). The power supply used has to be selected accordingly. In most applications the power consumption will be, however, significantly lower.

Attention:	
	With high load at the headers on the MBa335x the output voltage of the VCC3V3 regulator might be out of the specified range. In such a case a 2-regulator design should be used. The output voltage of the VCC12V regulator deviates significantly from the nominal value when high loads are switched on or off. The requirements for VCC12V, as well as the suitability of the regulator have to be checked with customer designs.

The parameters in the following Table 19, Table 20, and Table 21 apply to the switching regulators LTC3727, LT3503 and TPS5450.

Table 19: Parameter LTC3727 (VCC3V3 & VCC5V)

Parameter	Min.	Typ.	Max.	Unit	Remark
VCC3V3					
Output voltage	3.30	–	3.326	V	DC load
Output current	–	–	7.5	A	
Ripple	– –	49 46	– –	mV_{pp} mV_{pp}	(I_{OUT} = 2.5 A) (I_{OUT} = 7.5 A)
Load step change – add load Drop Control time	 – –	 88 75	 – –	 mV µs	I_{OUT} = 50 mA ⇨ 5 A
Load step change – remove load overshot Control time	 – –	 92 200	 – –	 mV µs	I_{OUT} = 5 A ⇨ 50 mA
VCC5V					
Output voltage	4.942	–	4.999	V	DC load
Output current	–	–	7	A	
Ripple	– –	39 40	– –	mV_{pp} mV_{pp}	(I_{OUT} = 2.3 A) (I_{OUT} = 7 A)
Load step change – add load drop Control time	 – –	 134 100	 – –	 mV µs	I_{OUT} = 150 mA ⇨ 5 A
Load step change – remove load overshot Control time	 – –	 127 250	 – –	 mV µs	I_{OUT} = 5 A ⇨ 150 mA

Table 20: Parameter TPS5450 (VCC12V)

Parameter	Min.	Typ.	Max.	Unit	Remark
Output voltage	12.058	–	12.061	V	DC load
Output current	–	–	3	A	
Ripple	– –	20 20	– –	mV_{pp} mV_{pp}	(I_{OUT} = 1 A) (I_{OUT} = 3 A)
Load step change – add load drop Control time	 – –	 1.5 0.5	 – –	 V ms	I_{OUT} = 0 A ⇨ 2 A
Load step change – remove load overshot Control time	 – –	 0.7 20	 – –	 V µs	I_{OUT} = 2 A ⇨ 0 A

Table 21: Parameter LT3503 (VCC1V5)

Parameter	Min.	Typ.	Max.	Unit	Remark
Output voltage	1.492	–	1.501	V	DC load
Output current	–	–	0.75	A	
Ripple	– –	6 8	– –	mV_{pp} mV_{pp}	(I_{OUT} = 0.375 A) (I_{OUT} = 0.75 A)
Load step change – add load drop Control time	 – –	 50 20	 – –	 mV µs	I_{OUT} = 20 mA ⇨ 0.75 A
Load step change – remove load overshot Control time	 – –	 30 20	 – –	 mV µs	I_{OUT} = 0.75 A ⇨ 20 mA

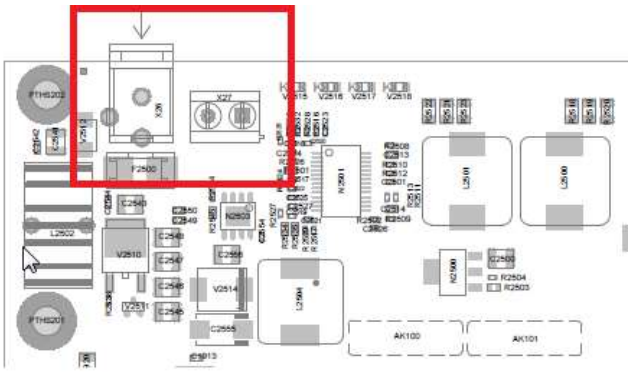


Illustration 11: Position of connectors X26, X27

Table 22: Power supply connectors

Manufacturer / Number	Description	Package
Cui Stack / PJ-102BH	DC jack 2.5 mm / 5.5 mm, nominal: 5 A / 24 V	THT3
Lumberg / KRM2	2-pin screw terminal, 250 V / 15 A	THT2

4.2 Communication interfaces

4.2.1 USB 2.0 Hi-Speed Host

A USB hub provides five USB 2.0 Hi-Speed host interfaces. The hub provides an upstream port and seven downstream ports. The USB connectors are supplied with 5 V by power distribution switches. The components used, provide current monitoring and can switch off the bus voltage with overload and/or overheat. The USB2517 is clocked by an external 24 MHz oscillator. USB host 1 and 2 are routed to a stacked USB Type-A connector (X7). USB host 3 is routed to a single Type-A connector (X8). USB host 4 is available at header X4 on the MBa335x and USB host 6 at header X5 on the MBa335x. USB host 5 is available at LVDS-CMD connector X18, USB host 7 is available at the Mini PCIe interface X22 (both on the bottom side of the MBa335x).

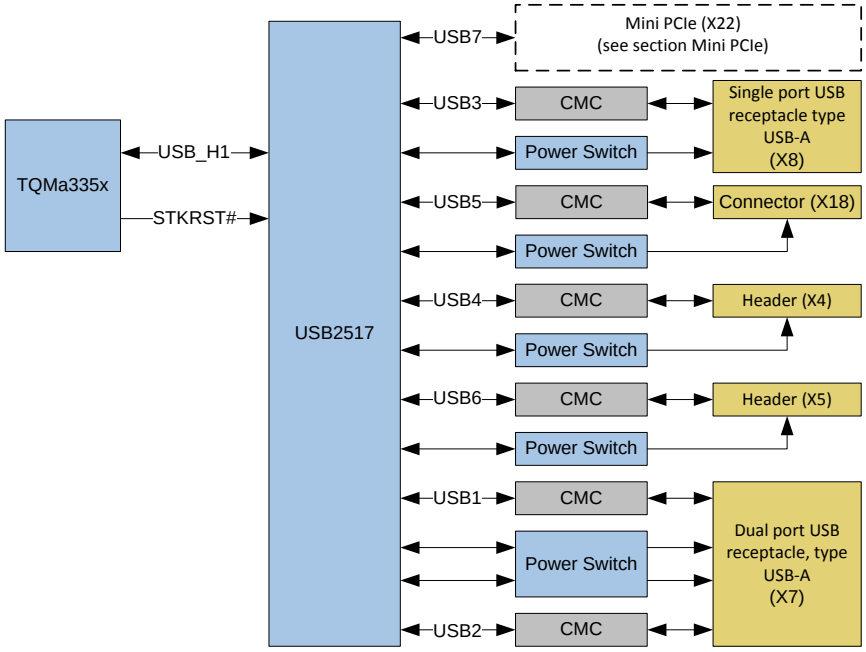


Illustration 12: Block diagram USB-Hub

The USB host port of the TQMa335x provides a theoretical data rate of 480 Mbit/s. The data rate is shared amongst the connected ports. The data rates of the ports can significantly deviate depending on the hardware and software used.

Table 23: Characteristics USB

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5.00	5.25	V	
Current	–	500	900	mA	

Attention:	
	The "Uniflash tool" provided by TI cannot be used with the MBa335x, because USB0 is not directly routed to a plug connector, but to a USB hub.

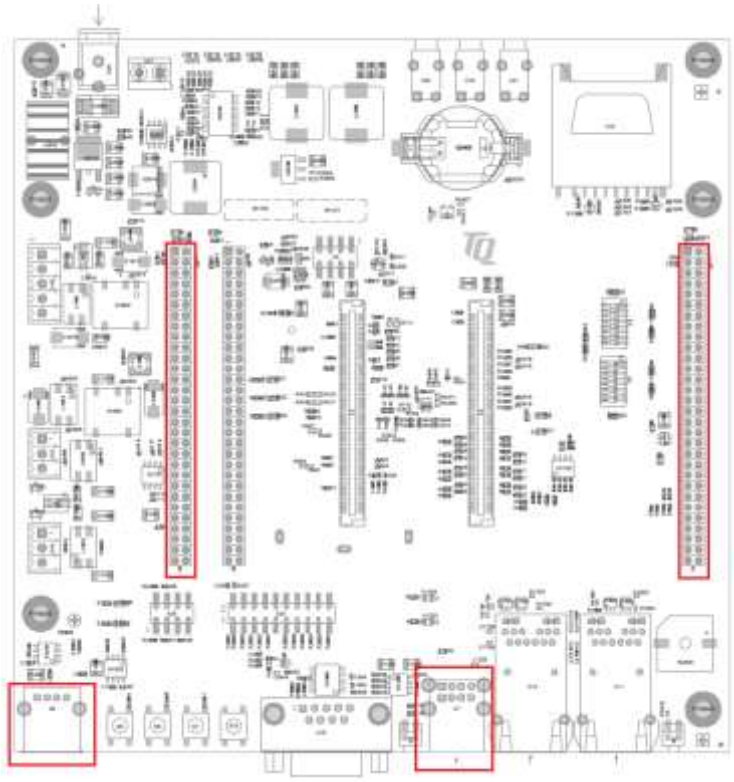


Illustration 13: Position of USB, X4, X5, X7, X8

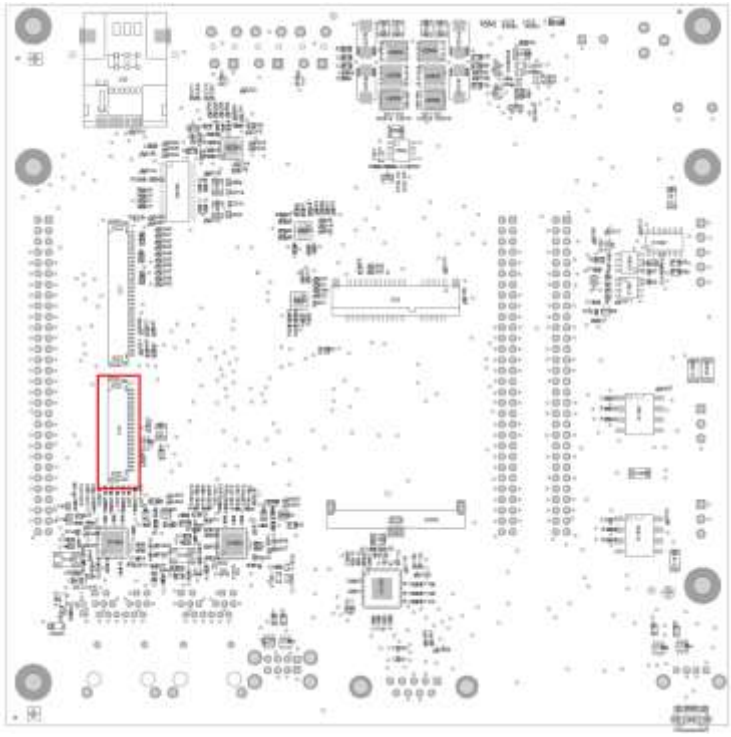


Illustration 14: Position of LVDS-CMD, X18

Table 24: USB Hub, components

Manufacturer / Number	Description	Package
Yamaichi / USB-A-002A	Dual port USB receptacle, type USB-A, U_N=30 V AC_{RMS} / I_N=1 A	THT8
Molex / 67643-2910	Single port USB receptacle type USB-A, U_N=30 V / I_N=1.5 A	THT4
Hirose / DF19G-20P-1H	Board-to-Cable connector 20-pin, 1 mm pitch	SMT20
Fischer Elektronik / SL 22 124 60 G	Header, 2.54 mm pitch, 2 × 30 pins	THT30

Table 25: Pinout USB-Host 1 and 2, X7

Pin	Pin name	Signal	Dir.	Remark
1A	VBUS	USB_H1_VBUS	P	100 µF to DGND; EMI filter
2A	D–	USB_H1_D_N	I/O	Common mode choke in series
3A	D+	USB_H1_D_P	I/O	Common mode choke in series
4A	DGND	DGND	P	
1B	VBUS	USB_H2_VBUS	P	100 µF to DGND; EMI filter
2B	D–	USB_H2_D_N	I/O	Common mode choke in series
3B	D+	USB_H2_D_P	I/O	Common mode choke in series
4B	DGND	DGND	P	
M1-4	DGND	DGND	P	

Table 26: Pinout USB-Host 3, X8

Pin	Pin name	Signal	Dir.	Remark
1A	VBUS	USB_H3_VBUS	P	100 µF to DGND; EMI filter
2A	D–	USB_H3_D_N	I/O	Common mode choke in series
3A	D+	USB_H3_D_P	I/O	Common mode choke in series
4A	DGND	DGND	P	
M1-2	DGND	DGND	P	

Table 27: Pinout USB-Host 5, X18

Pin	Pin name	Signal	Dir.	Remark
11	VBUS	USB_H5_VBUS	P	100 µF to DGND; EMI filter
13	D–	USB_H5_D_N	I/O	Common mode choke in series
14	D+	USB_H5_D_P	I/O	Common mode choke in series

Table 28: Pinout USB-Host 7, X22

Pin	Pin name	Signal	Dir.	Remark
36	D–	USB_H4_D_N	I/O	Common mode choke in series
38	D+	USB_H4_D_P	I/O	Common mode choke in series

4.2.2 USB 2.0 Hi-Speed OTG

The USB OTG interface of the TQMa335x is provided on the MBa335x. The OTG compatibility is maintained by a 5-pin Micro-AB connector. The ID signal is directly routed to the CPU.

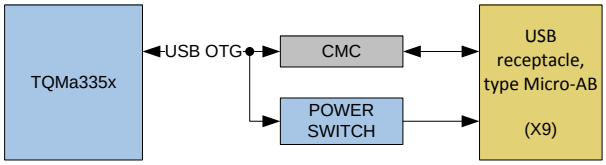


Illustration 15: Block diagram USB 2.0 Hi-Speed OTG

The interface can be a client or a host. To use this feature the appropriate software support is however necessary.
The OTG port provides a theoretical data rate of 480 Mbit/s. The data rate can significantly deviate depending on the hardware and software used.

Table 29: Characteristics USB OTG

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5.00	5.25	V	
Current	–	500	900	mA	

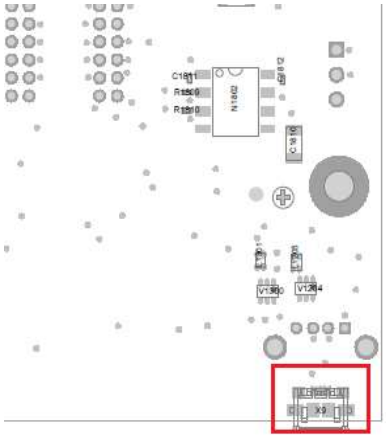


Illustration 16: Position of USB OTG X9

Table 30: USB Hub, component

Manufacturer / Number	Description	Package
TE Connectivity / 1981584-1	USB receptacle, angled, type Micro-AB	SMT8

Table 31: Pinout USB-Host OTG, X9

Pin	Pin name	Signal	Dir.	Remark
1	VBUS	USB_OTG_VBUS	P	100 µF to DGND; EMI filter, I_{max} = 100 mA
2	D–	USB_OTG_D_N	I/O	Common mode choke in series
3	D+	USB_OTG_D_P	I/O	Common mode choke in series
4	ID	USB_OTG.ID	I	
5	DGND	DGND	P	
M1-6	DGND	DGND	P	

4.2.3 Ethernet 1000BASE-T

The MBa335x provides two identical Gigabit Ethernet interfaces. A Micrel KSZ9031 PHY is used in each case. The RJ45 jacks X11 and X12 each contain integrated magnetics and two status LEDs. The PHY automatically selects speed (10/100/1000 Mbps) and mode (full-duplex / half-duplex). It meets IEEE 802.3 and provides options as for example Wake-on-LAN or jumbo frame support.

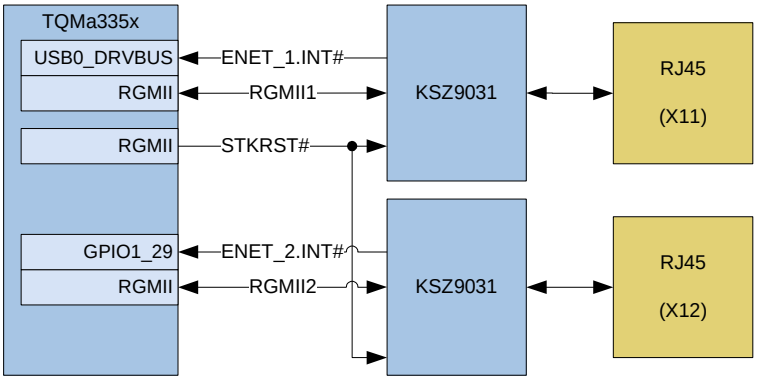


Illustration 17: Block diagram Ethernet 1000BASE-T

The interrupt outputs of the PHYs are routed to the TQMa335x by default. Optionally the interrupt outputs can be routed to the input port expander D901. See section 4.1.6 and the following table.

Table 32: Placement options for PHY interrupt

Option	R917	R924	R918	R923
ENET_1.INT# at USB0_DRVBUS (Default)	NP	0 Ω	x	
ENET_1.INT# at IO6 of D901	0 Ω	NP		
ENET_2.INT# at GPIO1_29 (Default)	x		NP	0 Ω
ENET_2.INT# at IO7 of D901			0 Ω	NP

Attention:	
	The PHY can only operate in master mode on account of PHY errata (ITEM #2). No link can be established if the remote station also only works in master mode.

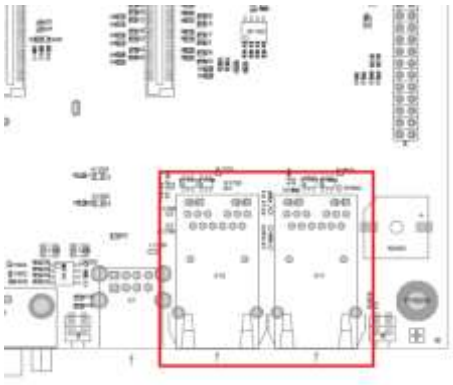


Illustration 18: Position of X11 and X12

Table 33: Ethernet 1000BASE-T, component

Manufacturer / Number	Description	Package
Pulse / JK0-0145NL	RJ45 receptacle, 10/100/1000BASE-T, integrated magnetics	THT16

Table 34: Pinout X11

Pin	Pin name	Signal	Dir.	Remark
1	DGND	DGND	P	100 nF to DGND
2	D3–	ETH1G_1_D3_N	I/O	
3	D3+	ETH1G_1_D3_P	I/O	
4	D2+	ETH1G_1_D2_P	I/O	
5	D2–	ETH1G_1_D2_N	I/O	
6	DGND	DGND	P	100 nF to DGND
7	DGND	DGND	P	100 nF to DGND
8	D4+	ETH1G_1_D4_P	I/O	
9	D4–	ETH1G_1_D4_N	I/O	
10	D1–	ETH1G_1_D1_N	I/O	
11	D1+	ETH1G_1_D1_P	I/O	
12	DGND	DGND	P	100 nF to DGND
13	LED	ETH1G_1_LED1	–	220 Ω in series, Activity, yellow (blinks at transfer)
14	LED	VCC3V3	–	
15	LED	ETH1G_1_LED2	–	220 Ω in series, Link, green (lights up when connected)
16	LED	VCC3V3	–	
17	VCC+	n.c.	–	
18	VCC–	n.c.	–	
M1-2	DGND	DGND	P	

Table 35: Pinout X12

Pin	Pin name	Signal	Dir.	Remark
1	DGND	DGND	P	100 nF to DGND
2	D3–	ETH1G_2_D3_N	I/O	
3	D3+	ETH1G_2_D3_P	I/O	
4	D2+	ETH1G_2_D2_P	I/O	
5	D2–	ETH1G_2_D2_N	I/O	
6	DGND	DGND	P	100 nF to DGND
7	DGND	DGND	P	100 nF to DGND
8	D4+	ETH1G_2_D4_P	I/O	
9	D4–	ETH1G_2_D4_N	I/O	
10	D1–	ETH1G_2_D1_N	I/O	
11	D1+	ETH1G_2_D1_P	I/O	
12	DGND	DGND	P	100 nF to DGND
13	LED	ETH1G_2_LED1	–	220 Ω in series, Activity, yellow (blinks at transfer)
14	LED	VCC3V3	–	
15	LED	ETH1G_2_LED2	–	220 Ω in series, Link, green (lights up when connected)
16	LED	VCC3V3	–	
17	VCC+	n.c.	–	
18	VCC–	n.c.	–	
M1-2	DGND	DGND	P	

4.2.4 CAN

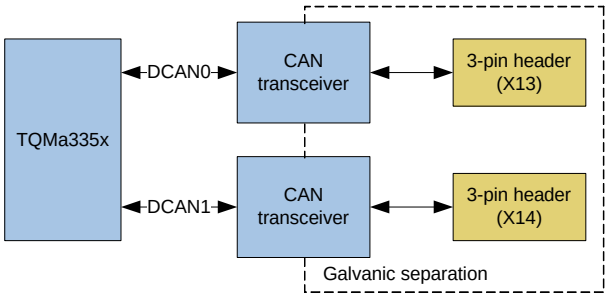


Illustration 19: Block diagram CAN

Both CAN interfaces of the MBa335x are directly connected to the CAN ports of the TQMa335x and are made available at the 3-pin connectors X13 and X14. Both interfaces are galvanically separated.
The CAN interfaces are galvanically not separated among themselves.
Die insulation voltage is 500 V_{RMS}[2]. A galvanically separated 5 V power supply is also provided.
The CAN signals can be terminated with 120 Ω using DIP switches S3-1 and S3-2.
The CAN interfaces are not qualified.

Table 36: CAN DIP switch settings, S3

Switch	Interface	ON	OFF
S3-1	CAN0	CAN1 terminated with 120 Ω	CAN1 not terminated
S3-2	CAN1	CAN2 terminated with 120 Ω	CAN2 not terminated

The following characteristics apply to the interfaces:

Table 37: Characteristics CAN

Parameter	Min.	Typ.	Max.	Unit	Remark
Transfer rate	–	–	1.0	Mbaud	
Electric strength	–	–	1	kV	RMS

RX and TX of DCAN1 can also be multiplexed as RTS# and CTS# for the RS-485 interface. In this case DCAN1 is not available. See the following table for the corresponding assembly options.

Table 38: Placement options for DCAN1_TX and DCAN1_RX

Signal	R416	R417	R418	R419
DCAN1_RX at DCAN1.RX	0 Ω	NP	X	
DCAN1_RX at UART0.RTS#	NP	0 Ω		
DCAN1_TX at DCAN1.TX	X		0 Ω	NP
DCAN1_TX at UART0.CTS#			NP	0 Ω

2: 500 V @60 Hz for 1 min; 1kV for 1 s.

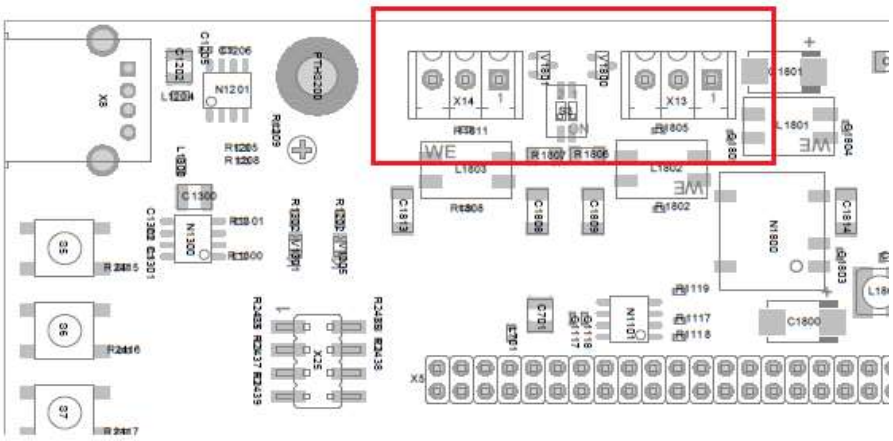


Illustration 20: Position of CAN connectors and DIP switch, X13, X14, S3

Table 39: CAN connectors

Manufacturer / Number	Description	Package
Phoenix Contact / MCV 1,5/ 3-G-3,5	3-pin housing, 160 V / 8 A, 3.5 mm pitch	THT3

Table 40: Pinout CAN0, X13

Pin	Signal	Dir.	Remark
1	CAN0_H_p	I/O	Galvanically separated
2	CAN0_L_n	I/O	Galvanically separated
3	DGND_CAN	P	Galvanically separated

Table 41: Pinout CAN1, X14

Pin	Signal	Dir.	Remark
1	CAN1_H_p	I/O	Galvanically separated
2	CAN1_L_n	I/O	Galvanically separated
3	DGND_CAN	P	Galvanically separated

4.2.5 RS-485

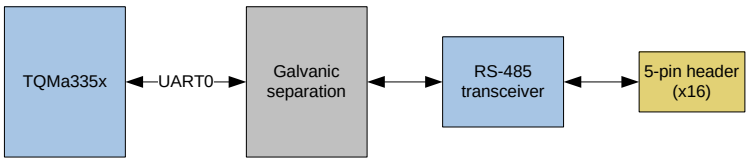


Illustration 21: Block diagram RS-485, X16

The UART0 interface of the TQMa335x is routed to an RS-485 transceiver (SP491), which provides the signals at the 9-pin D-Sub connector X16. The RS-485 interface is galvanically separated.

Die insulation voltage is 500 V_{RMS}[3]. A galvanically separated 5 V power supply is also provided.

In full-duplex mode the interface can operate with a maximum data rate of 1 Mbit/s. With an assembly option half-duplex is also possible.

Table 42: RS-485 mode settings

Mode	R1912	R1913	Remark
Full-duplex	NP	0 Ω	Receiver always active (default)
Half-duplex	0 Ω	NP	Receiver controlled by RTS# (UART0.RTS#)

The RS-485 signals can be terminated with 120 Ω using DIP switches S4-1 and S4-2.

Table 43: RS-485 DIP switch settings, S4

Switch	ON	OFF
S4-1	Receive path terminated with 120 Ω	Receive path not terminated
S4-2	Transmit path terminated with 120 Ω	Transmit path not terminated

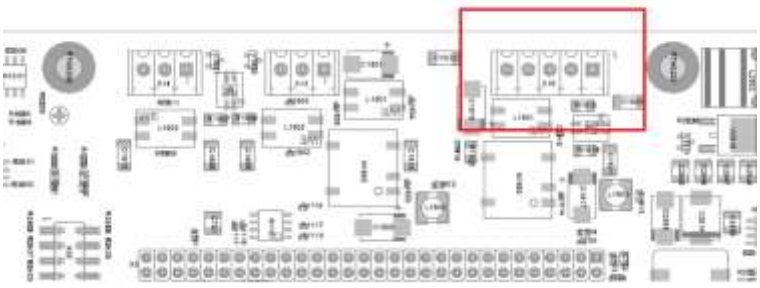


Illustration 22: Position of RS-485, X16

Table 44: RS-485 connector

Manufacturer / Number	Description	Package
Phoenix Contact / MCV1,5/5-G-3,5	5-pin housing , 160 V / 8 A, 3.5 mm pitch	THT5

Table 45: Pinout RS-485, X16

Pin	Signal	Dir.	Remark
1	RS-485_A	I	Galvanically separated
2	RS-485_B	I	Galvanically separated
3	RS-485_Y	O	Galvanically separated
4	RS-485_Z	O	Galvanically separated
5	DGND_RS-485	P	Galvanically separated

3: 500 V @60 Hz for 1 min; 1kV for 1 s.

4.2.6 RS-232

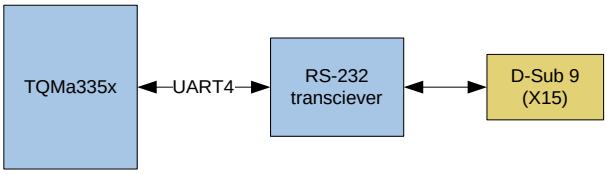


Illustration 23: Block diagram RS-232, X15

The UART4 interface of the TQMa335x is routed to transceiver SP3222E, which provides the signals according to the EIA/TIA-232-F Standard at the 9-pin D-Sub connector X15. The handshake signals RTS# and CTS# are also available at X15.

The UART4 interface is used to output debug information.

Additional information (e.g.: default baud rate) can be found in the TQMa335x Support-Wiki.

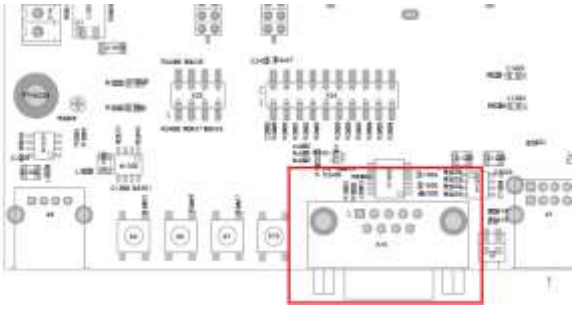


Illustration 24: Position of RS-232, X15

Table 46: RS-232, component

Manufacturer / Number	Description	Package
Yamaichi / DRA-09P11-ZN	9-pin D-Sub connector	THT9

Table 47: Pinout RS-232, X15

Pin	Pin name	Signal	Dir.	Remark
1	DCD	n.c.	–	Not used
2	RXD	RS-232_RXD	I	
3	TXD	RS-232_TXD	O	
4	DTR	n.c.	–	Not used
5	DGND	DGND	P	
6	DSR	n.c.	–	Not used
7	RTS	RS-232_RTS#	O	
8	CTS	RS-232_CTS#	I	
9	RI	n.c.	–	Not used
M1-2	DGND	DGND	P	

4.2.7 LVDS

The parallel LCD data bus of the TQMa335x is converted to a differential bus using an LVDS transmitter.
A clock pair and four data pairs are provided at the 30-pin FFC (X17). 3.3 V and 5 V are also provided at the connector.

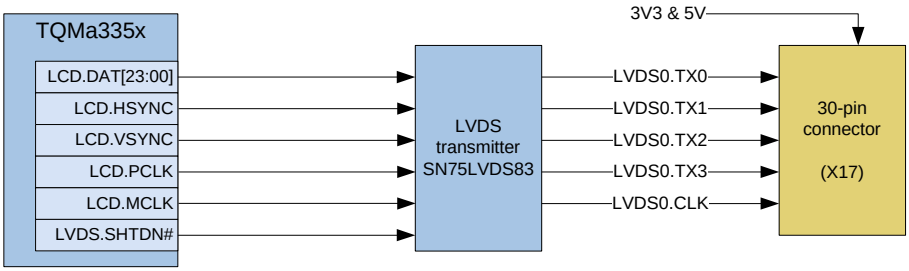


Illustration 25: Block diagram LVDS, X17

The LVDS transmitter can be switched off using LVDS.SHTDN#.

Illustration 26: Position of LVDS, X17

Table 48: LVDS connector, component

Manufacturer / Number	Description	Package
Hirose / DF19G-30P-1H	Board-to-Cable FFC connector, 30-pin, 1 mm pitch	SMT30

Table 49: Pinout LVDS, X17

Pin	Pin name	Signal	Dir.	Remark
1	0_TX0–	LVDS0_TX0_N	O	ESD filter
2	0_TX0+	LVDS0_TX0_P	O	ESD filter
3	0_TX1–	LVDS0_TX1_N	O	ESD filter
4	0_TX1+	LVDS0_TX1_P	O	ESD filter
5	0_TX2–	LVDS0_TX2_N	O	ESD filter
6	0_TX2+	LVDS0_TX2_P	O	ESD filter
7	DGND	DGND	P	
8	0_CLK–	LVDS0_CLK_N	O	ESD filter
9	0_CLK+	LVDS0_CLK_P	O	ESD filter
10	0_TX3–	LVDS0_TX3_N	O	ESD filter
11	0_TX3+	LVDS0_TX3_P	O	ESD filter
12	1_TX0–	n.c.	O	
13	1_TX0+	n.c.	O	
14	DGND	DGND	P	
15	1_TX1–	n.c.	O	
16	1_TX1+	n.c.	O	
17	DGND	DGND	P	
18	1_TX2–	n.c.	O	
19	1_TX2+	n.c.	O	
20	1_CLK–	n.c.	O	
21	1_CLK+	n.c.	O	
22	1_TX3–	n.c.	O	
23	1_TX3+	n.c.	O	
24	DGND	DGND	P	
25	VCC5V	VCC5V_LVDS	P	I_{max} = 1 A (excluding the current drawn from the headers) 11 µF to Ground; ferrite in series
26	VCC5V	VCC5V_LVDS	P	
27	VCC5V	VCC5V_LVDS	P	
28	VCC3V3	VCC3V3_LVDS	P	I_{max} = 1 A (excluding the current drawn from the headers) 11 µF to Ground; ferrite in series
29	VCC3V3	VCC3V3_LVDS	P	
30	VCC3V3	VCC3V3_LVDS	P	
M1-2	DGND	DGND	P	

4.2.8 LVDS-CMD

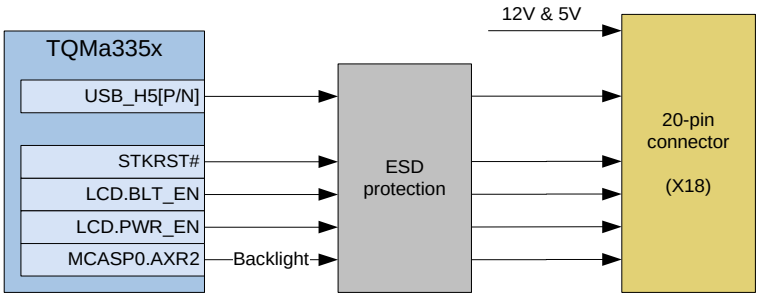


Illustration 27: Block diagram LVDS-CMD, X18

The LVDS-CMD connector X18 placed next to the LVDS connector X17 provides control signals for reset and backlight of an LCD as well as a 5 V and 12 V power supply. It also provides a USB interface. The TQMa335x provides several signals to control the backlight. The different signals can be selected with an assembly option. MCASP0.AXR2 is the default. See Table 50 for the available signals and the required component placement.

Table 50: Placement option for LCD contrast

Signal	R928	R929	R930	R931	R932	R933
GPIO2.0	0 Ω	NP	NP	NP	NP	NP
TIMER.4	NP	0 Ω	NP	NP	NP	NP
TIMER.5	NP	NP	0 Ω	NP	NP	NP
TIMER.6	NP	NP	NP	0 Ω	NP	NP
TIMER.7	NP	NP	NP	NP	0 Ω	NP
MCASP0.AXR2, (Default)	NP	NP	NP	NP	NP	0 Ω

Attention:	
	Depending on the assembly option the available signals can also be used for other functions. The configuration should be selected unambiguously.

The characteristics in section 4.2.1 also apply to the USB interface.

Table 51: Characteristics LVDS-CMD

Parameter	Min.	Typ.	Max.	Unit	Remark
Current at 12 V	–	–	1	A	
Current at 5 V	–	–	1	A	

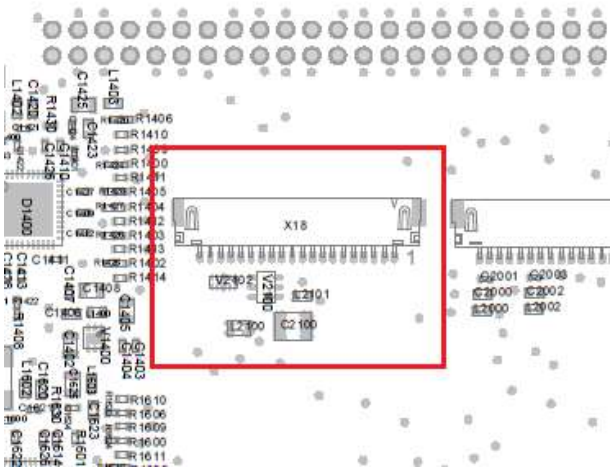


Illustration 28: Position of LVDS-CMD, X18

Table 52: LVDS-CMD connector

Manufacturer / Number	Description	Package
Hirose / DF19G-20P-1H	Board-to-Cable FFC connector 20-pin, 1 mm pitch	SMT20

Table 53: Pinout LVDS CMD, X18

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	I_{max} = 1 A (excluding the current drawn from the headers) 11 µF to Ground
2	VCC12V	VCC12V	P	
3	VCC12V	VCC12V	P	
4	DGND	DGND	P	
5	DGND	DGND	P	
6	DGND	DGND	P	
7	VCC5V	VCC5V	P	I_{max} = 1 A (excluding the current drawn from the headers) 11 µF to Ground
8	VCC5V	VCC5V	P	
9	DGND	DGND	P	
10	DGND	DGND	P	
11	VBUS	USB_H5_VBUS	P	100 µF to DGND + EMI filter
12	DGND	DGND	P	
13	D–	USB_H5_D_N	I/O	Common mode choke in series, ESD filter
14	D+	USB_H5_D_P	I/O	Common mode choke in series, ESD filter
15	DGND	DGND	P	
16	LCD_RESET	STKRST#	O	
17	LCD_BL_EN	LCD.BLT_EN	O	
18	LCD_PWR_EN	LCD.PWR_EN	O	
19	LCD_CONTRAST	LCD.CONTRAST	O	
20	DGND	DGND	P	
M1-2	DGND	DGND	P	

4.2.9 Audio

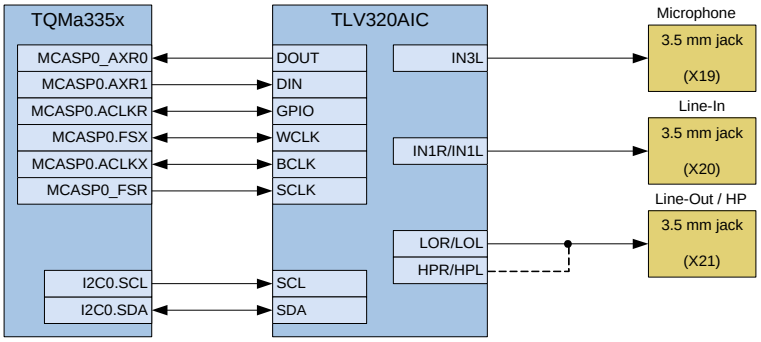


Illustration 29: Block diagram audio

Audio input and output is available using the audio codec TLV320AIC. The codec is connected via the MCASP0 interface of the AM335x. The MBa335x provides a stereo line-in, a stereo line-out and a microphone input as well as a headphone output with integrated amplifier.

An assembly option selects between line-out and headphone. The following table shows the possible configuration.

Table 54: Configuration line-out / headphone, X21

Mode	R2207	R2209	R2210	R2211	Remark
Headphone	NP	NP	0 Ω	0 Ω	
Line-out	0 Ω	0 Ω	NP	NP	Default

The following tables show the characteristics of the audio codec.

Table 55: Characteristics of audio and headphone, X21

Parameter	Min.	Typ.	Max.	Unit	Remark
Load resistor	14.4	16	–	Ω	Single-ended configuration
Load resistor	24.4	32	–	Ω	Differential configuration
Output power	–	64	–	mW	At 16 Ω input impedance and –40 dB THD
Output power	–	40	–	mW	At 32 Ω input impedance and –40 dB THD
Signal-noise ratio	87	100	–	dB	

Table 56: Characteristics of line-out, X21

Parameter	Min.	Typ.	Max.	Unit	Remark
Load resistor	0.6	106	–	kΩ	
Signal-noise ratio	87	100	–	dB	

Table 57: Characteristics of line-in, X20

Parameter	Min.	Typ.	Max.	Unit	Remark
Signal-noise ratio	80	93	–	dB	

Table 58: Characteristics of microphone, X19

Parameter	Min.	Typ.	Max.	Unit	Remark
Output Noise	–	10	–	μV_{RMS}	
Current	–	3	–	mA	

Some signals of the MCASP interface share functions with the EMU interface. The interface is selected with the assembly options in Table 70 to Table 72. Two signals of the TQMa335x are available as audio-clock, which are selected by assembly option (see section 4.2.12).

Table 59: Configuration of Line-Out or Headphone, X21

Clock	R2203	R2205	Remark
CLKOUT.1	0 Ω	NP	Default
CLKOUT.2	NP	0 Ω	

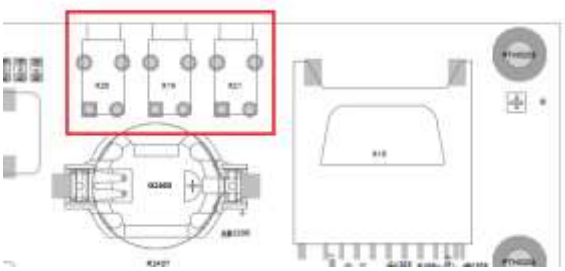


Illustration 30: Position of audio jacks X19, X20, X21

Table 60: Audio, component

Manufacturer / Number	Description	Package
Yamaichi / LJE3530K	Jack 3.5 mm	THT4

Table 61: Pinout microphone, X19

Pin	Pin name	Signal	Dir.	Remark
1	Ground	AGND_AUDIO	P	
2A,2B	Left	MIC_IN	I	2.2 kΩ in series to MIC_BIAS + ESD protection
3	Right	AGND_AUDIO	I	10 kΩ in series, right channel not used (only mono)

Table 62: Pinout line-in, X20

Pin	Pin name	Signal	Dir.	Remark
1	Ground	AGND_AUDIO	P	
2A,2B	Left	LINE_IN_L	I	470 nF in series + ESD protection
3	Right	LINE_IN_R	I	470 nF in series + ESD protection

Table 63: Pinout line-out, X21

Pin	Pin name	Signal	Dir.	Remark
1	Ground	AGND_AUDIO	P	
2A,2B	Left	AUDIO_OUT_L	O	1 µF and 100 Ω in series + 47 nF to AGND_AUDIO + ESD protection optional connection to HP_L is possible
3	Right	AUDIO_OUT_R	O	1 µF and 100 Ω in series + 47 nF to AGND_AUDIO + ESD protection optional connection to HP_R is possible

4.2.10 SD card

The SD card slot is directly connected to the MMC0 interface of the TQMa335x.
An optional resistor is integrated in series in the clock line to adjust the line attenuation.

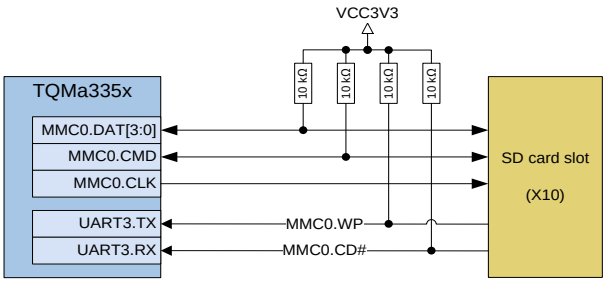


Illustration 31: Block diagram SD card slot, X10

It is possible to boot from SD card (see section 4.3.5).
The read and write speeds of the SD card interface depend on the SD card used.
The maximum available data rate is to be taken from the respective CPU Reference Manual.

Attention:	
	The signals WP and CD# are not routed to the SD card connector by default. This may cause transmission errors and it is recommended to assemble R402 and R405 in such a case to use these signals at the SD card interface. In this case the UART3 interface is not available.

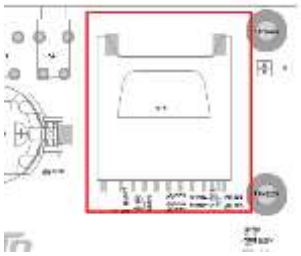


Illustration 32: Position of SD card slot, X10

Table 64: SD card connector

Manufacturer / Number	Description	Package
Yamaichi / FPS009-2405-0	SD/MMC card connector	SMD9

Table 65: Pinout SD card, X10

Pin	Pin name	Signal	Dir.	Remark
1	CD/DAT3/CS	MMC0.DAT3	I/O	
2	CMD/DI	MMC0.CMD	I/O	10 kΩ to VCC3V3
3	VSS1	DGND	P	
4	VDD	VCC3V3	P	110 µF to DGND
5	CLK	MMC0.CLK_R	O	0 Ω in series
6	VSS2	DGND	P	
7	DAT0/DO	MMC0.DAT0	I/O	
8	DAT1	MMC0.DAT1	I/O	
9	DAT2	MMC0.DAT2	I/O	
CDS	CARD_DETECT	MMC0.CD#	I	10 kΩ to VCC3V3
COM	COMMON	DGND	P	
WP	WRITE_PROTECT	MMC0.WP	I	10 kΩ to VCC3V3
M1-2	DGND	DGND	P	

4.2.11 Mini PCIe

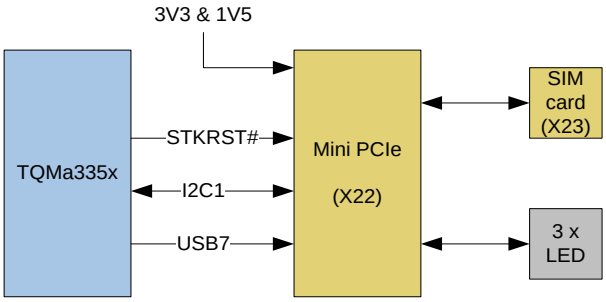


Illustration 33: Block diagram Mini PCIe

The MBa335x provides a Mini PCIe socket. It provides a USB, I²C and a SIM card interface.

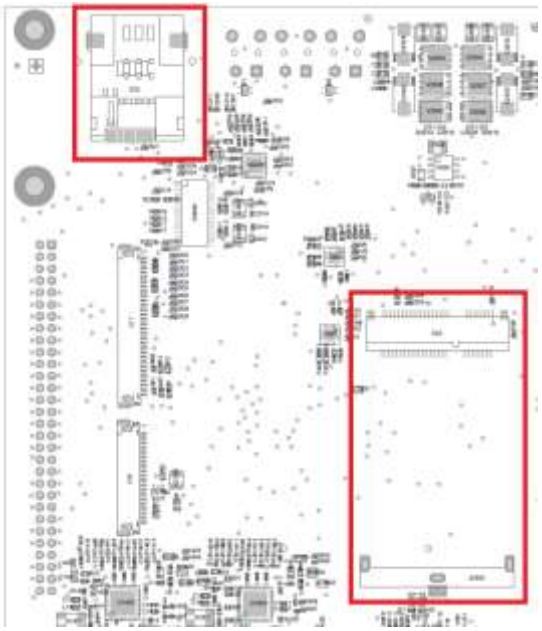


Illustration 34: Position of Mini PCIe, X22, X23

Table 66: Mini PCIe, components

Manufacturer / Number	Description	Package
Nexus / 5020HB56R	Mini PCIe connector	SMT54
Nexus / 5022M56R	Mini PCIe holder	THT3
YAMAICHI / FMS006Z-2101-0	SIM card holder	SMT10

Table 67: Pinout Mini PCIe, X22

Pin	Pin name	Signal	Dir.	Remark
1	WAKE#	PCIE.WAKE#	I	
2	3.3V	VCC3V3_MPCIE	P	Can be switched off by PCIE.PWR_EN
3	Reserved	n.c.	–	
4	GND	DGND	P	
5	Reserved	n.c.	–	
6	1.5V	VCC1V5	P	Can be switched off by PCIE.PWR_EN
7	CLKREQ#	n.c.	–	
8	Reserved	UIM_PWR	P	
9	GND	DGND	P	
10	Reserved	UIM_DATA	I/O	
11	REFCLK–	n.c.	–	
12	Reserved	UIM_CLK	O	
13	REFCLK+	n.c.	–	
14	Reserved	UIM_RST	O	
15	GND	DGND	P	
16	Reserved	UIM_VPP	P	
17	Reserved	n.c.	–	
18	GND	DGND	P	
19	Reserved	n.c.	–	
20	Reserved	PCIE.DIS#	I	
21	GND	DGND	P	
22	PERST#	STKRST#	I	
23	PERn0	n.c.	–	
24	+3.3Vaux	VCC3V3_MPCIE	P	Can be switched off by PCIE.PWR_EN
25	PERp0	n.c.	–	
26	GND	DGND	P	
27	GND	DGND	P	
28	+1.5V	VCC1V5	P	Can be switched off by PCIE.PWR_EN
29	GND	DGND	P	
30	SMB_CLK	I2C1.SCL	I	
31	PETn0	n.c.	–	
32	SMB_DATA	I2C1.SDA	I/O	
33	PETp0	n.c.	–	
34	GND	DGND	P	
35	GND	DGND	P	
36	USB_D–	USB_H7_D_N	I/O	Common mode choke in series
37	Reserved	DGND	P	
38	USB_D+	USB_H7_D_P	I/O	Common mode choke in series
39	Reserved	VCC3V3_MPCIE	P	Can be switched off by PCIE.PWR_EN
40	GND	DGND	P	
41	Reserved	VCC3V3_MPCIE	P	Can be switched off by PCIE.PWR_EN
42	LED_WWAN#	LED_WWAN#	I	Connected to LED
43	Reserved	DGND	P	
44	LED_WLAN#	LED_WLAN#	I	Connected to LED
45	Reserved	n.c.	–	
46	LED_WPAN#	LED_WPAN#	I	Connected to LED
47	Reserved	n.c.	–	
48	+1.5V	VCC1V5	P	Can be switched off by PCIE.PWR_EN
49	Reserved	n.c.	–	
50	GND	DGND	P	
51	Reserved	n.c.	–	
52	+3.3V	VCC3V3_MPCIE	P	Can be switched off by PCIE.PWR_EN

Table 68: Pinout SIM card, X23

Pin	Pin name	Signal	Dir.	Remark
C1	VCC	UIM_PWR	P	
C2	RST	UIM_RST	I	
C3	CLK	UIM_CLK	I	
C5	GND	DGND	P	
C6	VPP	UIM_VPP	P	
C7	I/O	UIM_DATA	I/O	
SW1-2	–	n.c.	–	

4.2.12 JTAG & EMU

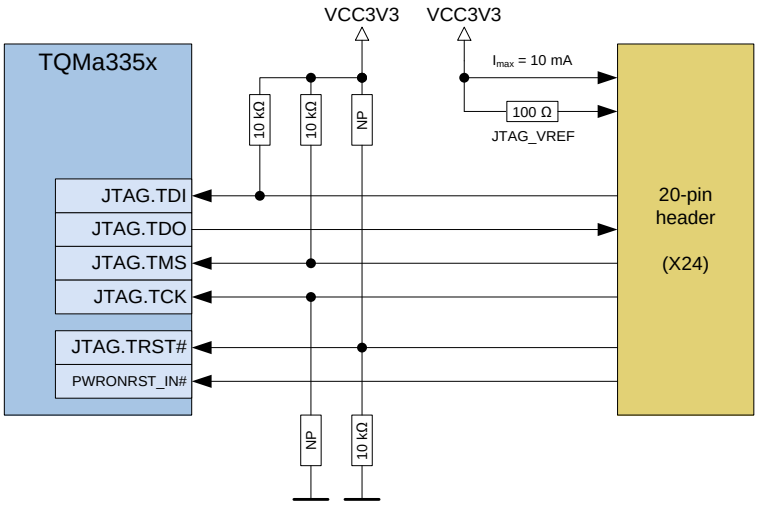


Illustration 35: Block diagram JTAG

The JTAG interface is routed to a 20-pin header (X24). The pull-ups/downs required for the signals TDI, TMS, TRST# and TCK are assembled on the MBa335x and can partly be reconfigured. All signals use 3.3 V as a reference. The JTAG interface has no ESD protection.

The TQMa335x can be reset via JTAG. PWRONRST_IN# is used as reset input for the TQMa335x by default. The configuration can be changed according to Table 69.

Table 69: Reset source for JTAG-Reset

Option	R431	R432
JTAGRST# an WARMRST#	0 Ω	NP
JTAGRST# an PWRONRST_IN# (default)	NP	0 Ω

In addition to the JTAG signals at X24 five EMU signals are available at X25. These signals are partially multiplexed with other functions, e.g. the MCASP (audio) interface. Table 70 to Table 72 show the assembly options. EMU0 and EMU1 define the JTAG mode.

Table 70: Reset source for EMU.2

Option	R406	R407
MCASP0_FSR an MCASP0.FSR (default)	0 Ω	NP
MCASP0_FSR an EMU.2	NP	0 Ω

Table 71: Reset source for EMU.4

Option	R408	R409
MCASP0_AXR3 an MCASP0.AXR3 (default)	0 Ω	NP
MCASP0_AXR3 an EMU.4	NP	0 Ω

Table 72: Reset source for EMU.3

Option	R410	R411
MCASP0_AXR1 an MCASP0.AXR1 (default)	0 Ω	NP
MCASP0_FSR an EMU.3	NP	0 Ω

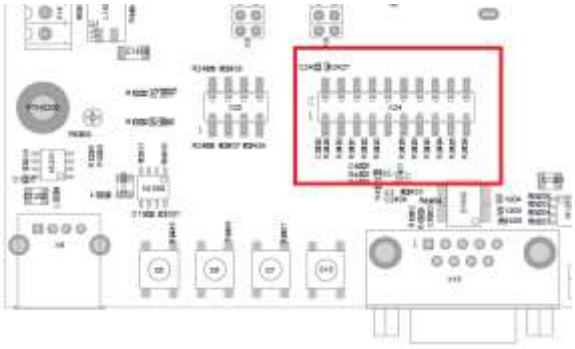


Illustration 36: Position of JTAG, X24

Table 73: JTAG connector

Manufacturer / Number	Description	Package
Fischer Elektronik / SL-11-SMD-052-20-G-BTR	Header, 2.54 mm pitch, 2 × 10 pins	SMD20

Table 74: Pinout JTAG, X24

Pin	Signal	Dir.	Remark
1	JTAG.VREF	P	100 Ω to VCC3V3, use only as reference
2	VCC3V3	P	0 Ω to VCC3V3, I_{max} = 10 mA
3	JTAG.TRST#	I	10 kΩ Pull-Up to VCC3V3
4	DGND	P	
5	JTAG.TDI	I	10 kΩ Pull-Up to VCC3V3
6	DGND	P	
7	JTAG.TMS	I	10 kΩ Pull-Up to VCC3V3
8	DGND	P	
9	JTAG.TCK	I	22 Ω in series
10	DGND	P	
11	JTAG.RTCK	I	22 Ω to pin 9
12	DGND	P	
13	JTAG.TDO	O	22 Ω in series
14	DGND	P	
15	JTAG.SRST#	I	10 kΩ Pull-Up to VCC3V3; via buffer to JTAGRST#
16	DGND	P	
17	VCC3V3	P	10 kΩ Pull-Up to VCC3V3
18	DGND	P	
19	DGND	P	10 kΩ to DGND
20	DGND	P	

4.2.13 Headers X4, X5, X6

All unused as well as other signals are routed to the headers X4, X5, X6 on the MBa335x, to permit a comprehensive evaluation of the TQMa335x modules. All headers are 60-pin with 2.54 mm pitch.
The headers are positioned in such a way, that adaptor boards which additional electronics and connectors can be plugged in.

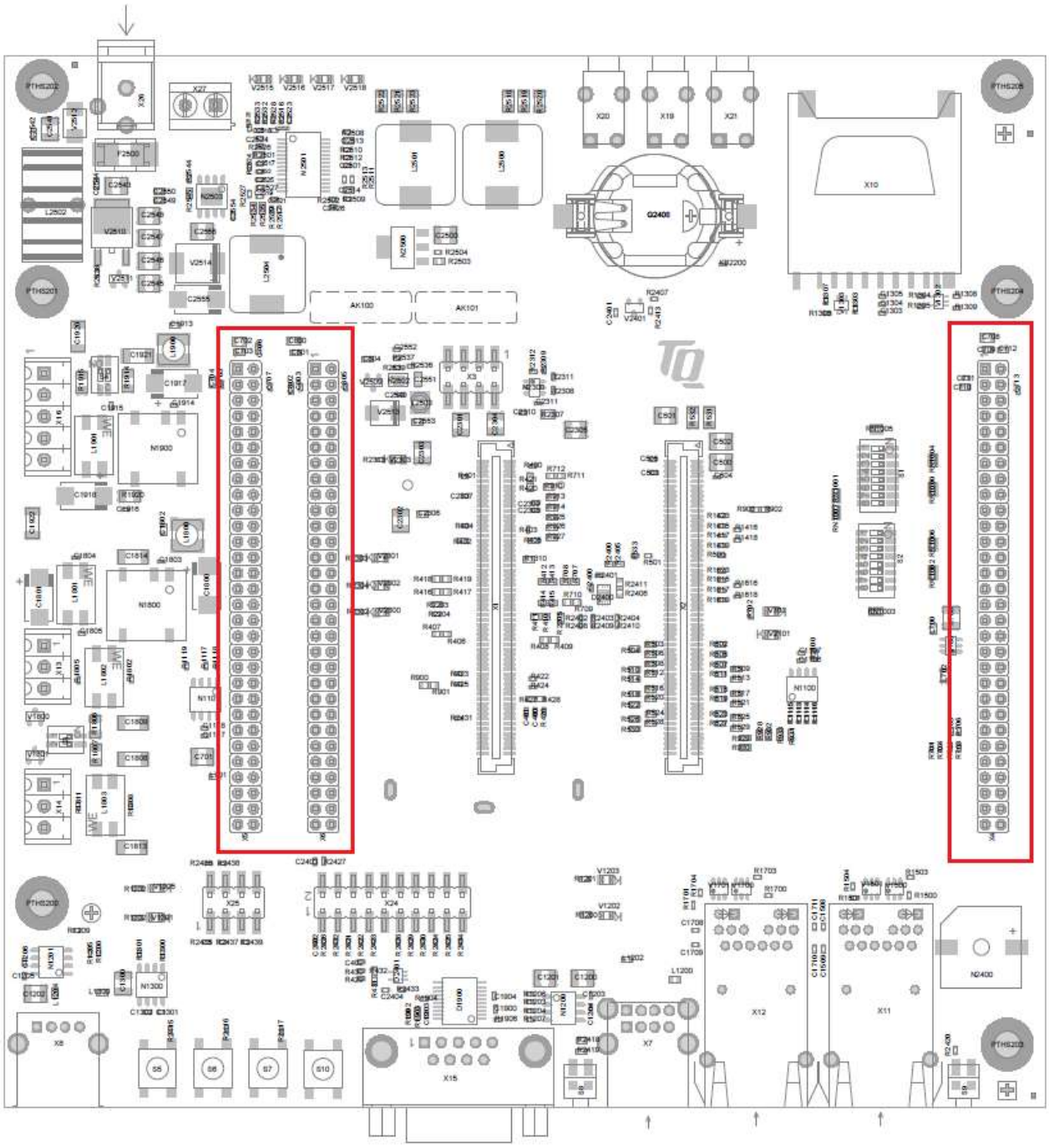


Illustration 37: Position of headers X4, X5, X6

Table 75: Headers, component

Manufacturer / Number	Description	Package
Fischer Elektronik / SL 22 124 60 G	Header, 2.54 mm pitch, 2 × 30 pins	THT30

Table 76: Pinout header 1, X4

Pin	Interface	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	111 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
2	VCC3V3	VCC3V3	P	11 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
3	VCC5V	VCC5V	P	11 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
4	VCC3V3	VCC3V3	P	11 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
5	DGND	DGND	P	
6	DGND	DGND	P	
7	LCD	LCD.PCLK	O	
8	LCD	LCD.AC_BIAS_EN#	O	
9	LCD	LCD.HSYNC	O	
10	LCD	LCD.DAT11	O	
11	LCD	LCD.VSYNC	O	
12	LCD	LCD.DAT13	O	
13	LCD	LCD.DAT17	O	
14	LCD	LCD.DAT15	O	
15	LCD	LCD.DAT12	O	
16	LCD	LCD.DAT6	O	
17	LCD	LCD.DAT14	O	
18	LCD	LCD.DAT8	O	
19	LCD	LCD.DAT5	O	
20	LCD	LCD.DAT10	O	
21	LCD	LCD.DAT7	O	
22	LCD	LCD.DAT0	O	
23	LCD	LCD.DAT9	O	
24	LCD	LCD.DAT2	O	
25	LCD	LCD.DAT16	O	
26	LCD	LCD.DAT4	O	
27	LCD	LCD.DAT1	O	
28	LCD	LCD.DAT23	O	
29	LCD	LCD.DAT3	O	
30	LCD	LCD.DAT20	O	
31	LCD	LCD.DAT22	O	
32	LCD	LCD.DAT19	O	
33	LCD	LCD.DAT21	O	
34	USB	USB_H4_VBUS	P	100 µF to DGND + EMI filter + LED
35	LCD	LCD.DAT18	O	
36	USB	USB_H4_D_N	I/O	Common mode choke in series
37	DGND	DGND	P	
38	USB	USB_H4_D_P	I/O	Common mode choke in series
39	I2C1	I2C1.SCL	O	
40	DGND	DGND	P	
41	I2C1	I2C1.SDA	I/O	
42	SPI1	SPI1.CS0	O	
43	SPI1	SPI1.MOSI	O	
44	SPI1	SPI1.MISO	I	
45	–	n.c.	–	
46	SPI1	SPI1.SCLK	O	
47	LCD	LCD.MCLK	O	
48	DGND	DGND	P	
49	LCD	LCD.PWR_EN	O	Pull-Down or Pull-Up can be assembled
50	LCD	LCD.BLT_EN	O	Pull-Down or Pull-Up can be assembled
51	Diverse	STKRST	O	
52	LCD	LCD.CONTRAST	O	
53	DGND	DGND	P	
54	DGND	DGND	P	
55	Touch	Touch Y+	AIN	
56	Touch	Touch X+	AIN	
57	Touch	Touch Y–	AIN	
58	Touch	ANALOG.AIN1	AIN	
59	DGND	DGND	P	
60	DGND	DGND	P	

Table 77: Pinout header 2, X5

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	111 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
2	VCC3V3	VCC3V3	P	11 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
3	VCC5V	VCC5V	P	11 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
4	VCC3V3	VCC3V3	P	11 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
5	DGND	DGND	P	
6	DGND	DGND	P	
7	ADC	ANALOG.AIN4	AIN	
8	ADC	ANALOG.AIN0	AIN	
9	ADC	ANALOG.AIN5	AIN	
10	ADC	ANALOG.AIN1	AIN	
11	ADC	ANALOG.AIN6	AIN	
12	ADC	ANALOG.AIN2	AIN	
13	ADC	ANALOG.AIN7	AIN	
14	ADC	ANALOG.AIN3	AIN	
15	DGND	DGND	P	
16	DGND	DGND	P	
17	TIMER	TIMER.4	I/O	
18	GPIO	GPIO1_28	I/O	
19	TIMER	TIMER.5	I/O	
20	GPIO	GPIO1_29	I/O	
21	TIMER	TIMER.6	I/O	
22	GPIO	GPIO2.0	I/O	
23	TIMER	TIMER.7	I/O	
24	DGND	DGND	P	
25	DGND	DGND	P	
26	CAN	DCAN0_TX	O	
27	TIMER	CLKOUT.1	O	
28	CAN	DCAN0_RX	I	
29	TIMER	CLKOUT.2	O	
30	CAN	DCAN1_TX	O	
31	–	n.c.	–	
32	CAN	DCAN1_RX	I	
33	DGND	DGND	P	
34	DGND	DGND	P	
35	SPI	SPI0.MOSI	O	
36	SPI	SPI0.MISO	I	
37	SPI	SPI0.SCLK	O	
38	SPI	SPI0.CS0	O	
39	DGND	DGND	P	
40	DGND	DGND	P	
41	UART	UART0.RX	I	
42	UART	UART0.TX	O	
43	DGND	DGND	P	
44	DGND	DGND	P	
45	UART	UART3.RX	I	
46	UART	UART3.TX	O	
47	DGND	DGND	P	
48	DGND	DGND	P	
49	UART	UART4.RX	I	
50	UART	UART4.TX	O	Unused USB signal line for USB_H (used for upstream port USB-Hub)
51	DGND	DGND	P	
52	DGND	DGND	P	Unused USB signal line for USB_H (used for upstream port USB-Hub)
53	USB	USB_H6_VBUS	P	
54	USB	USB0_DRVBUS	P	
55	USB	USB_H6.D_N	I/O	
56	USB	USB0_CE	O	
57	USB	USB_H6.D_P	I/O	
58	USB	USB1_CE	O	
59	DGND	DGND	P	
60	DGND	DGND	P	

Table 78: Pinout header 3, X6

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	111 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
2	VCC3V3	VCC3V3	P	11 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
3	VCC5V	VCC5V	P	11 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
4	VCC3V3	VCC3V3	P	11 µF to DGND, I_{max} = 1 A (excluding the current drawn from the headers)
5	DGND	DGND	P	
6	DGND	DGND	P	
7	N.C.[4]	RES1.SPARE1	–	
8	–	n.c.	–	
9	N.C.[4]	RES1.SPARE2	–	
10	–	n.c.	–	
11	N.C.[4]	RES1.SPARE3	–	
12	–	n.c.	–	
13	N.C.[4]	RES1.SPARE4	–	
14	–	n.c.	–	
15	N.C.[4]	RES2.SPARE1	–	
16	–	n.c.	–	
17	N.C.[4]	RES2.SPARE2	–	
18	–	n.c.	–	
19	N.C.[4]	RES2.SPARE3	–	
20	DGND	DGND	P	
21	DGND	DGND	P	
22	CONFIG	TEST.VDDS-DDR	P	
23	CONFIG	PWRONRST_IN#	I	
24	CONFIG	TEST.VDDS	P	
25	CONFIG	PWRONRST_OUT#	O	
26	CONFIG	TEST.VDD-PLL	P	
27	CONFIG	EXTINT#	I	
28	CONFIG	TEST.VDD-USB	P	
29	CONFIG	EXT_WAKEUP	I	
30	CONFIG	TEST.VDDA-ADC	P	
31	DGND	DGND	P	
32	CONFIG	TEST.VDDS-RTC	P	
33	I2C	I2C0.SDA	I/O	
34	CONFIG	TEST.VDD-CORE	P	
35	I2C	I2C0.SCL	O	
36	CONFIG	TEST.VDDS-MPU	P	
37	DGND	DGND	P	
38	DGND	DGND	P	
39	Power	VBACKUP_RTC	P	
40	Power	VBACKUP_PMIC	P	
41	CONFIG	PMIC_SLEEP	I	
42	CONFIG	PMIC_PWRON	I	
43	CONFIG	RTC_INT#	I	
44	CONFIG	PMIC_INT	O	
45	–	n.c.	–	
46	CONFIG	TEMP_OS#	O	
47	–	n.c.	–	
48	Power	VDDSHV3V3	P	
49	DGND	DGND	P	
50	DGND	DGND	P	
51	Audio	MCASP0.AXR0	I	
52	Audio	MCASP0.FSR	O	
53	Audio	MCASP0.AXR1	O	
54	Audio	MCASP0.FSX	I/O	
55	Audio	MCASP0.AXR2	I/O	
56	Audio	MCASP0.ACLKR	I/O	
57	Audio	MCASP0.AXR3	I/O	
58	Audio	MCASP0.ACLKX	I/O	
59	DGND	DGND	P	
60	DGND	DGND	P	

4: Connected with TQMa335x but not used internally.

4.3 Diagnose- and user interfaces

4.3.1 Diagnose LEDs

The MBa335x provides 18 diagnose LEDs to indicate the system condition.

Table 79: Meaning of diagnose LEDs

Function	Reference	Colour	Signal
Power	V2515	Green	24 V Power-LED (lights up when supply 24 V is active)
	V2516	Green	12 V Power-LED (lights up when supply 12 V is active)
	V2517	Green	5 V Power-LED (lights up when supply 5 V is active)
	V2518	Green	3.3 V Power-LED (lights up when supply 3.3 V is active)
USB	V1202	Green	VBUS USB Host 1 (lights up when VBUS of USB Host 1 is active)
	V1203	Green	VBUS USB Host 2 (lights up when VBUS of USB Host 2 is active)
	V1205	Green	VBUS USB Host 3 (lights up when VBUS of USB Host 3 is active)
	V1301	Green	VBUS USB OTG (lights up when VBUS of USB OTG is active)
	V2101	Green	VBUS USB Host 5 (LVDS-CMD, lights up when VBUS of USB Host 5 is active)
	V701	Green	VBUS USB Host 4 (header 1, lights up when VBUS of USB Host 4 is active)
Mini PCIe	V2300	Green	Mini PCIe WWAN
	V2301	Green	Mini PCIe WLAN
	V2302	Green	Mini PCIe WPAN
	V2303	Green	Mini PCIe 3.3 V Power-LED (lights up when PCIe supply 3.3 V is active)
Ethernet	X11B	Yellow	Activity-LED Ethernet 1 (blinks at transfer)
	X11C	Green	Link-LED Ethernet 1 (lights up when connected)
	X12B	Yellow	Activity-LED Ethernet 2 (blinks at transfer)
	X12C	Green	Link-LED Ethernet 2 (lights up when connected)

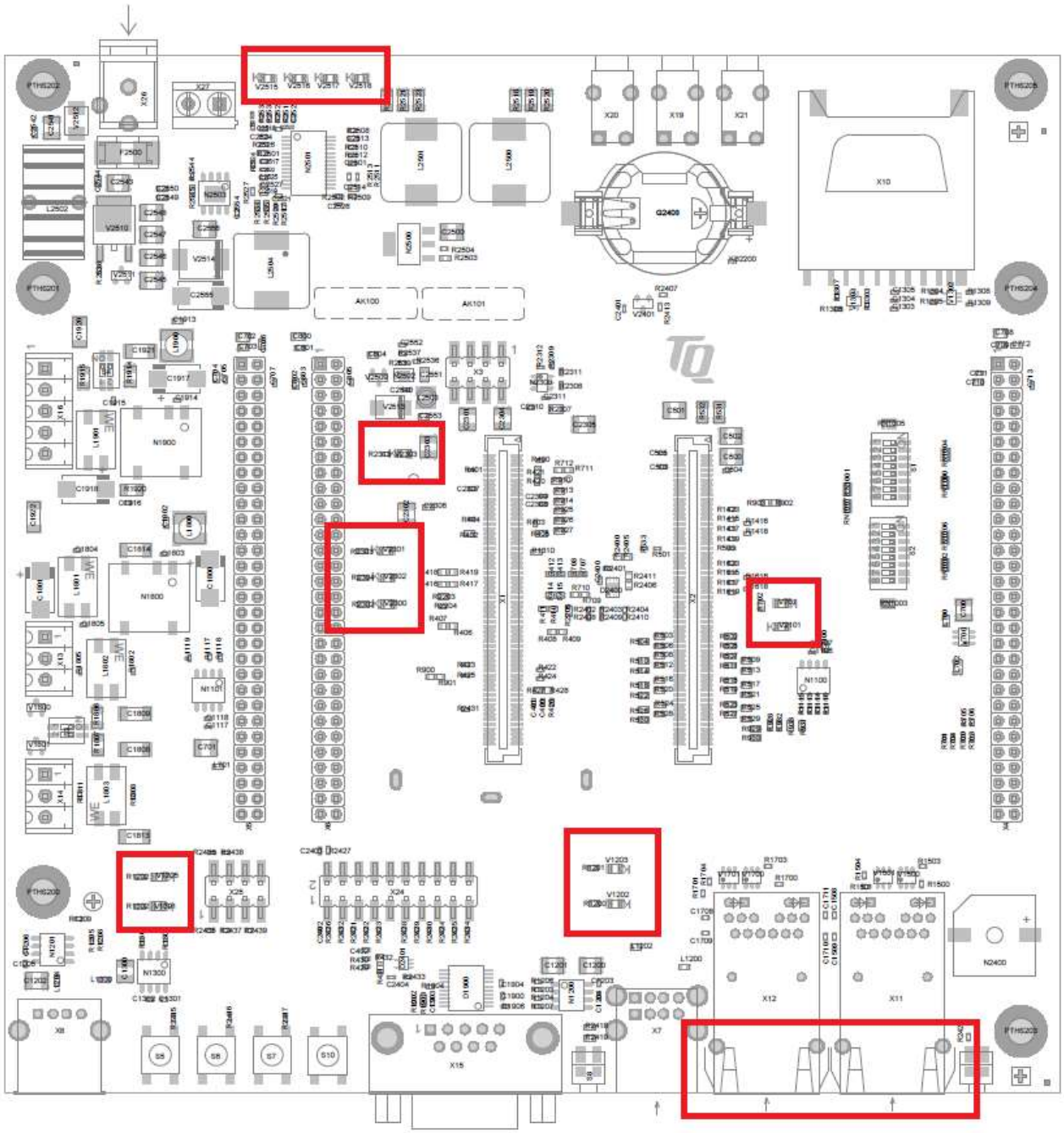


Illustration 38: Position of LEDs

Table 80: Status LEDs, component

Manufacturer / Number	Description	Package
Osram / LGR971-KN-1	SMD LED, green, chip 0805	SMT2

4.3.2 Navigation buttons

Three navigation buttons are available on the MBa335x for development purposes. They are routed to a port expander and can be read out by I2C0. The port expander registers the change of a push button signal at interrupt output GPIO1_28, which makes the debouncing unnecessary.

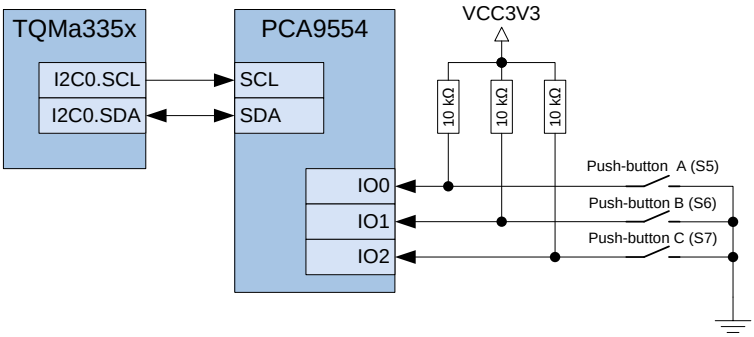


Illustration 39: Block diagram navigation buttons

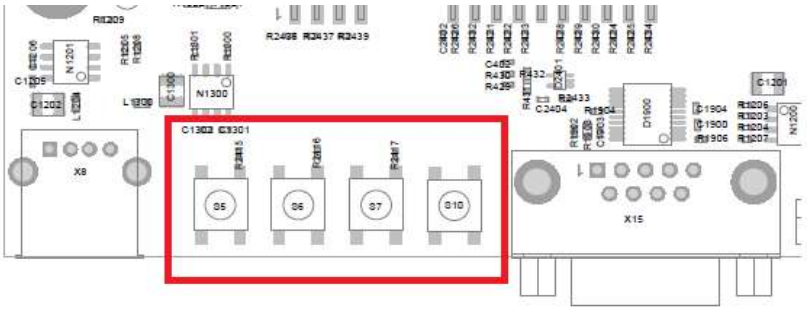


Illustration 40: Position of navigation buttons S5, S6, S7, S10

Table 81: Navigation buttons, component

Manufacturer / Number	Description	Package
Knitter switch / TSS 61N	Push button	SMT4

4.3.3 Power-On and Reset-button

For further information see section 4.1.5.

4.3.4 CAN and RS-485 termination

For further information see section 4.2.4 and 4.2.5.

4.3.5 Boot-Mode configuration

The TQMa335x can boot from different sources:

- eMMC (MMC1)
- SD card (MMC0)
- SPI NOR flash (SPI0)

Additional boot sources can be used according to the data sheet of the AM335x, insofar as this is possible with the respective pin usage.

The settings[5] of S1 and S2 define, which device is selected as primary boot source. The exact list of signals, as well as their meaning for the boot process, is to be taken from the TQMa335x User's Manual. Some of the signals are not relevant for boot source selection.

The AM335x supports so-called boot sequences, i.e. if it fails to boot from the first boot device, it tries to boot from the next boot device. See TQMa335x User's Manual for more details. Only the primary boot source is given in Table 82.

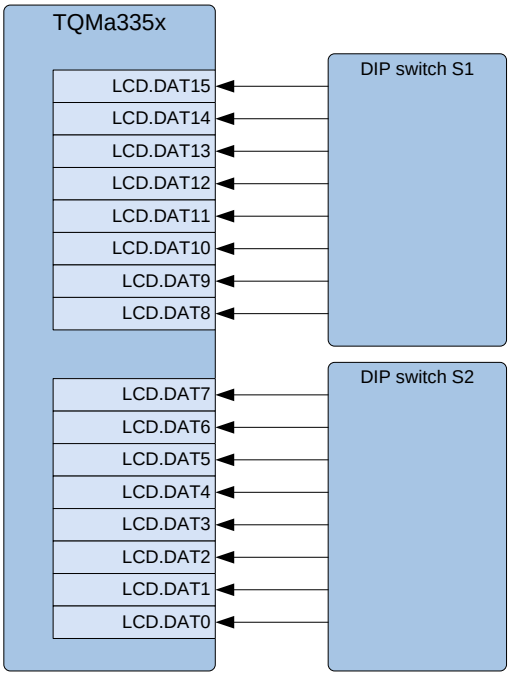


Illustration 41: Configuration of boot loader source with DIP switches S1 and S2

5: Only applies to TQMa335x modules with unburnt eFuses.

The following settings can be used as default, see also MBa335x DIP switch settings.

Table 82: Default boot-configuration

DIP switch	eMMC (MMC1)	SPI NOR flash (SPI0)	SD card (MMC0)
S1-1	x	x	x
S1-2	x	x	x
S1-3	x	x	x
S1-4	x	x	x
S1-5	x	x	x
S1-6	x	x	x
S1-7	1	1	1
S1-8	0	0	0
S2-1	0	0	1
S2-2	0	0	1
S2-3	1	0	1
S2-4	1	1	0
S2-5	1	1	1
S2-6	x	x	x
S2-7	x	x	x
S2-8	x	x	x

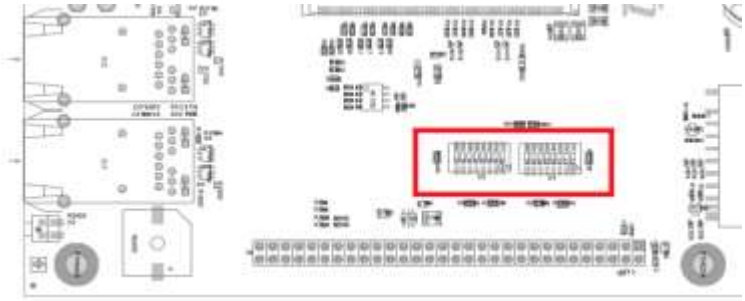


Illustration 42: Position of Boot-Mode configuration DIP switches S1, S2

Table 83: DIP switch, component

Manufacturer / Number	Description	Package
Nidec Copal / CHS-08TA	8-fold DIP switch, 1.27 mm pitch	SMT16

4.3.6 Buzzer

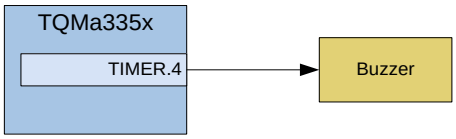


Illustration 43: Block diagram buzzer

The MBa335x provides a buzzer to signal acoustic events. The buzzer is directly controlled by a GPIO from the TQMa335x. Several signals of the TQMa335x are available, which can be selected with an assembly option. TIMER.4 is the default assembly. See following table for the available signals as well as the required assembly option.

Table 84: Placement option for buzzer control

Signal	R910	R913	R914	R925	R926	R927
GPIO2.0	0 Ω	NP	NP	NP	NP	NP
TIMER.4 (default)	NP	0 Ω	NP	NP	NP	NP
TIMER.5	NP	NP	0 Ω	NP	NP	NP
TIMER.6	NP	NP	NP	0 Ω	NP	NP
TIMER.7	NP	NP	NP	NP	0 Ω	NP
MCASP0.AXR2	NP	NP	NP	NP	NP	0 Ω

Attention:	
	Depending on the assembly option the available signals can also be used for other functions. The configuration should be selected unambiguously.

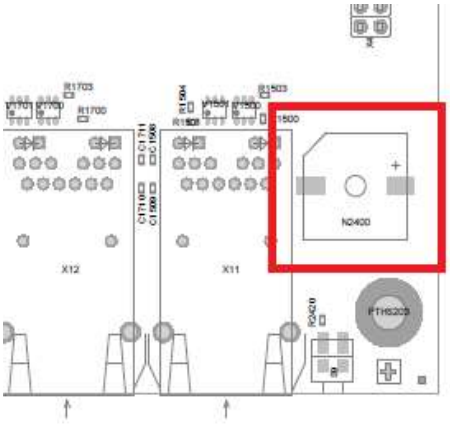


Illustration 44: Position of buzzer, N2400

Table 85: Buzzer, component

Manufacturer / Number	Description	Package
PUI Audio / SMI-1324-TW-5V-2-R	Buzzer, 5 V (typ.), 30 mA (max.)	SMD2

5. SOFTWARE-SPECIFICATION

No software is required for the MBa335x.
Suitable software is only required on the module TQMa335x and is not a part of this specification.
More information can be found in the Support Wiki for the TQMa335x.

6. MECHANICS

6.1 Dimensions

The overall dimensions (length × width) of the MBa335x are 170 × 170 mm².
The maximum height of the MBa335x is approximately 24.1 mm.
The MBa335x has six mounting holes with a diameter of 4.3 mm.
The MBa335x weighs approximately 227 g without TQMa335x.

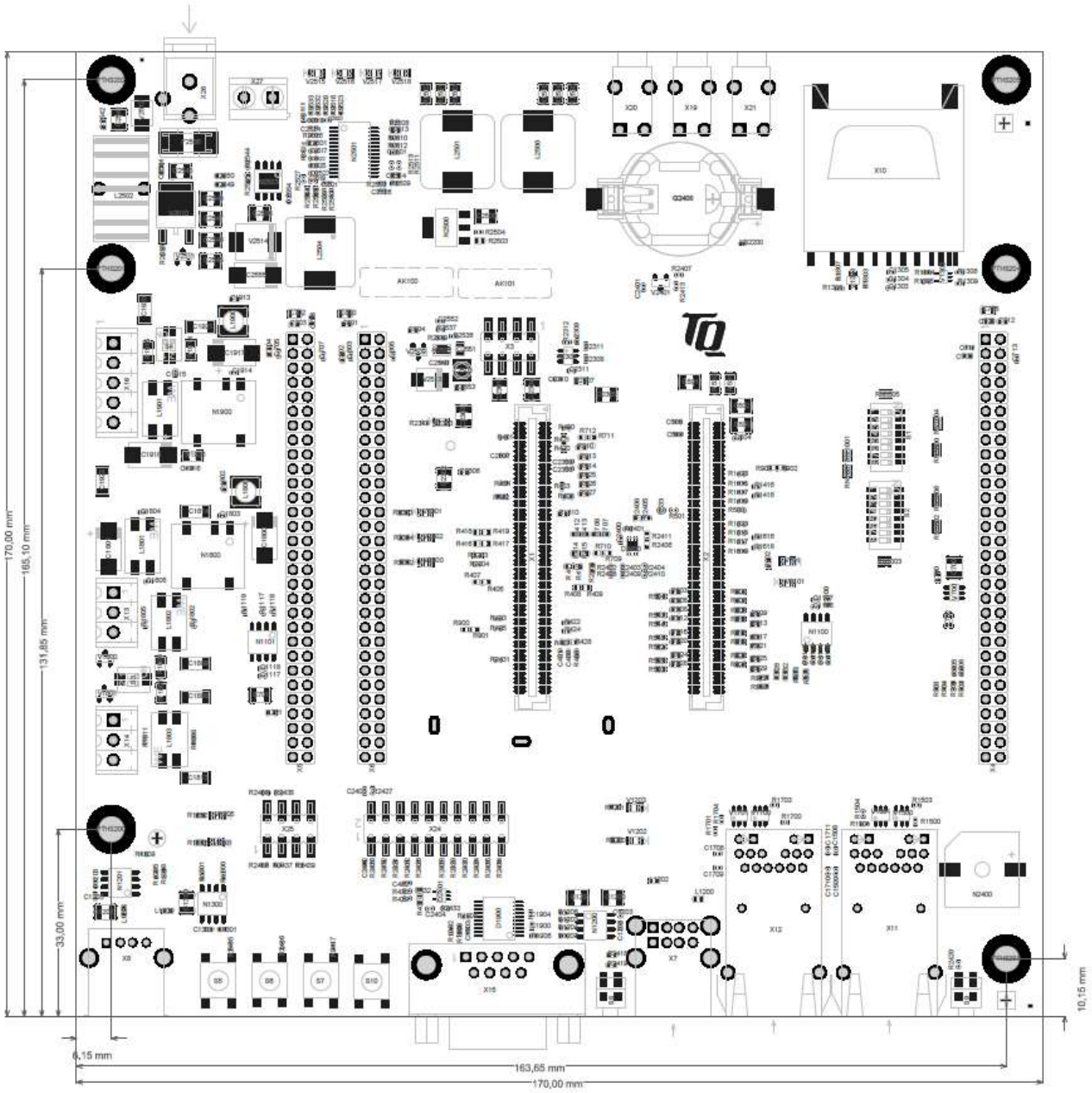


Illustration 45: MBa335x dimensions

6.2 Housing

The form factor and the mounting holes are designed for installation in the COMSys housing.

6.3 Thermal management

No special precautions were taken concerning the thermal management of the MBa335x.
Cooling the TQMa335x may be necessary depending on the software or the TQMa335x used.
More information is to be taken from the User's Manual of the TQMa335x.

6.4 Assembly

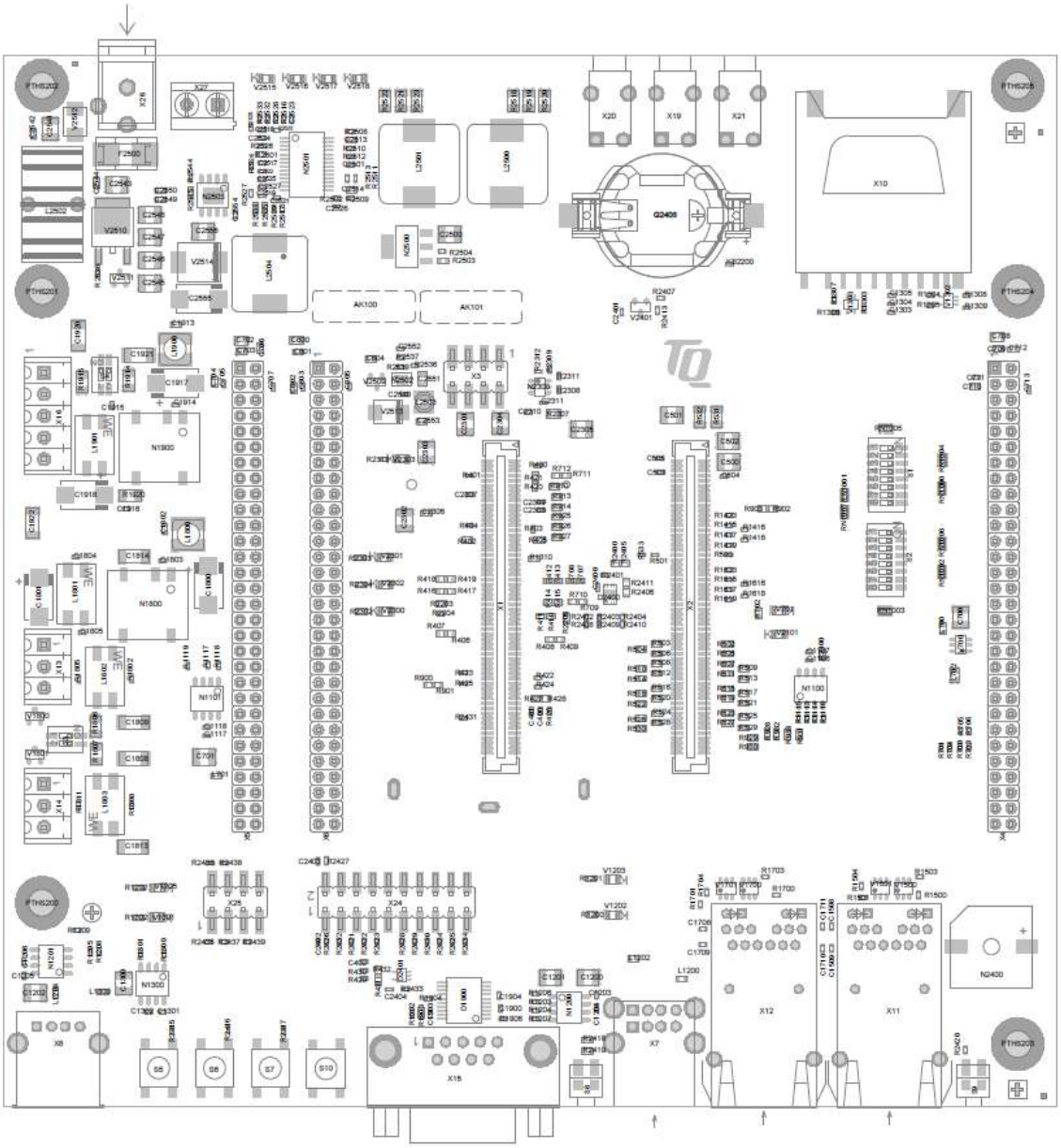


Illustration 46: Component placement top

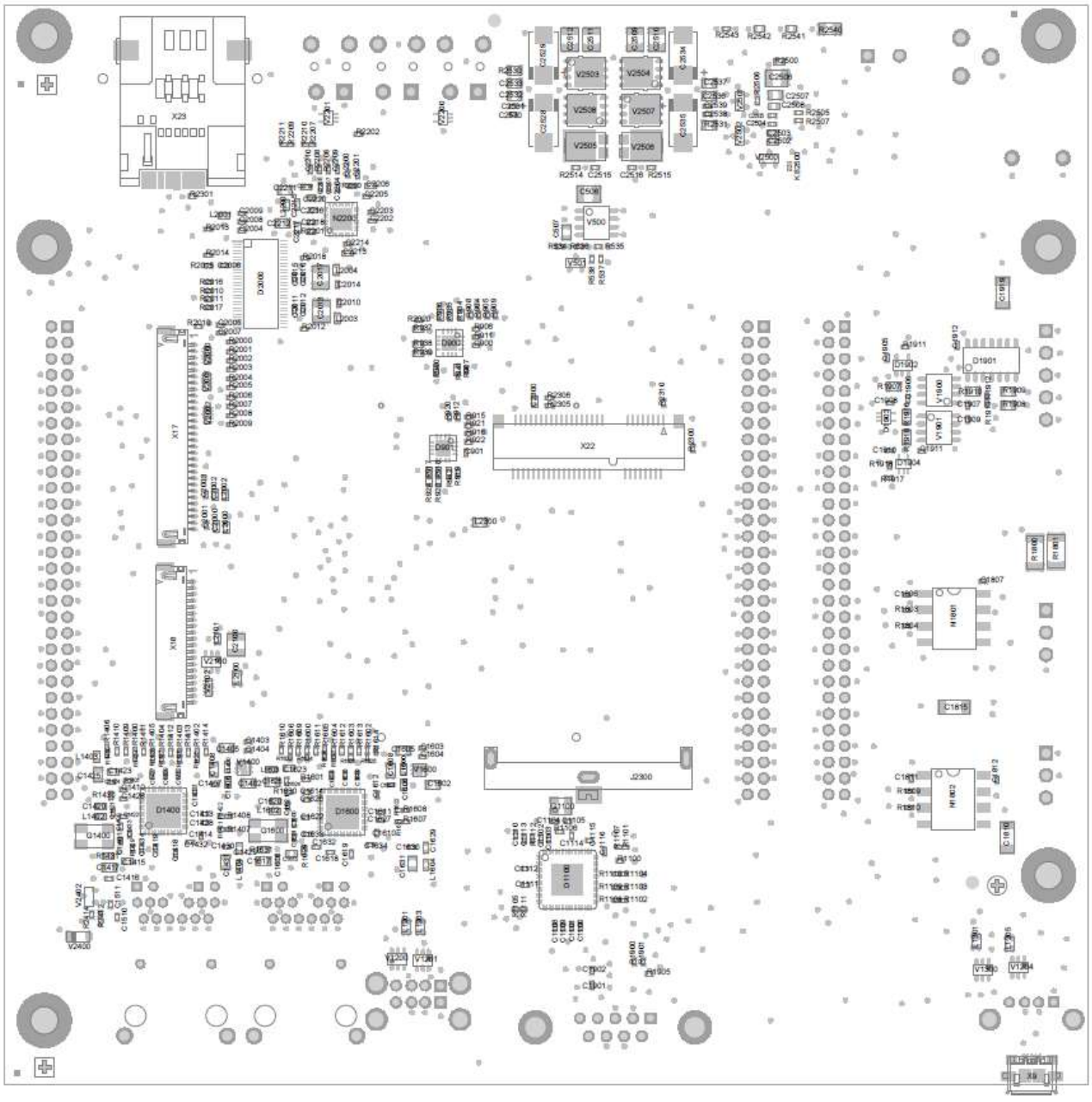


Illustration 47: Component placement bottom

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

Because the MBa335x is a development platform, no EMC specific tests have been carried out.
During the development of the MBa335x the following standard was taken into account:

- EMC-Interference radiation:
  Measurement of the electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 1 GHz according to DIN EN 55022 A1:2007.

7.2 ESD

Most of the interfaces on the MBa335x are protected against electrostatic discharge. [6]
The interfaces, which provide an ESD protection is to be taken from the circuit diagram.

7.3 Operational safety and personal security

Due to the occurring voltages (≤30 V DC), tests with respect to the operational and personal safety haven't been carried out.

8. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 86: Climatic and operational conditions MBa335x

Parameter	Range	Remark
Permitted environmental temperature	0 °C to 70 °C	Without Lithium battery
Permitted environmental temperature	0 °C to 60 °C	With Lithium battery
Permitted storage temperature	–10 °C to 60 °C	–
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Attention:	
	The CPU belongs to a performance category in which a cooling system may be essential in certain applications. It is the responsibility of the customer to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).

8.1 Protection against external effects

Protection class IP00 was defined for the MBa335x. There is no protection against foreign objects, touch or humidity.

8.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa335x. The MBa335x is designed to be insensitive to vibration and impact.

6: The JTAG interface has no ESD protection.

9. ENVIRONMENT PROTECTION

9.1 RoHS

The MBa335x is manufactured RoHS compliant.

- All components and assemblies used are RoHS compliant
- RoHS compliant soldering processes are used

9.2 WEEE

The company placing the product on the market is responsible for the observance of the WEEE regulation (TQ-Systems GmbH).
To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

9.3 REACH

The EU-chemical regulation 1907/2006 (REACH regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as TQ-Systems GmbH is informed by suppliers accordingly. Regarding REACH an examination exceeding RoHS verification was not carried out.

9.4 EuP

The guideline 2005/32/EC, also Energy using Products (EuP), is not applicable for the following reasons:

- The guideline is only applicable for products with an annual production quantity of >200,000
- The external power supply is a purchased part

9.5 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the MBa335x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.
The energy consumption of this subassembly is minimised by suitable measures. The MBa335x is delivered in reusable packaging.

9.6 Batteries

9.6.1 General notes

Due to technical reasons a battery is necessary for this product. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is unavoidable for technical reasons, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

9.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.
- During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

9.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
The energy consumption of this subassembly is minimised by suitable measures.
Printed pc-boards are delivered in reusable packaging.
Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, 1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

10. APPENDIX

10.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 87: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR3L	DDR3 Low Voltage
DIN	Deutsche Industrie Norm
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	European Standard (Europäische Norm)
ESD	Electrostatic Discharge
EuP	Energy using Products
FET	Field Effect Transistor
FFC	Flat Flex Cable
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
HP	Headphone
I/O	Input/Output
I²C	Inter-Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signal
MCASP	Multichannel Audio Serial Port
MII	Media Independent Interface
MMC	Multimedia Card
MSB	Most Significant Bit
MTBF	Mean operating Time Between Failures

Table 87: Acronyms (continued)

Acronym	Meaning
n.c.	Not Connected
NOR	Not-Or
NP	Not Placed
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industries Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PRU	Programmable Real-Time Unit
PU	Pull-Up
REACH	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ45	Registered Jack 45
RMS	Root Mean Square
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232	Recommended Standard (serial interface)
RS-485	Recommended Standard (serial interface)
RTC	Real-Time Clock
SD card	Secure Digital card
SD/MMC	Secure Digital Multimedia Card
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SMD	Surface-Mounted Device
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
THD	Through-Hole Device
THT	Through-Hole Technology
UART	Universal Asynchronous Receiver/Transmitter
UIM	User Identity Module
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WP	Write-Protection
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

10.2 References

Table 88: Further applicable documents

No.	Name	Revision / Date	Author	Company
[1]	TQMa335x User's Manual	Latest Revision	–	TQ-Systems GmbH
[2]	Data sheet TPS65910x	October 2014	–	Texas Instruments

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