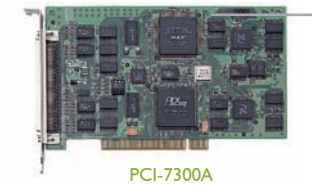
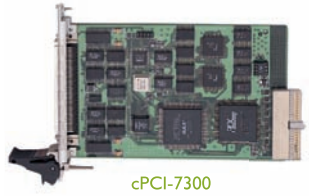
PCI/PCIe-7300A, cPCI-7300

80 MB/s High-Speed 32-CH Digital I/O Cards



PCI-7300A

PCIe-7300A



cPCI-7300

Introduction

ADLINK's PCI/PCIe-7300A and cPCI-7300 are ultra-highspeed digital I/O card consisting of 32 digital input/output channels. High performance designs and state-of-the-art technology make these cards ideal for a wide range of applications, such as high-speed data transfer, digital pattern generation and digital pattern capture applications, and logic analyzer applications. Trigger signals are available to start the data acquisition of pattern generation.

Maximum Data Acquisition Rate

For sustained data transfer directly from or to host memory, the maximum data acquisition rate can be 80 MB/s. The maximum data transfer rates between external device and onboard FIFO can be up to 80 MB/s for DO and 160 MB/s for DI. 80MB/s is achieved by 32-bit data width multiplied by an internal 20 MHz clock. 160 MB/s is achieved by 32-bit data width with an external 40 MHz clock for digital input channels only. The PCI/PCIe-7300A, cPCI-7300 can reach 160 MB/s throughput only when the acquired data length is less than FIFO size (16 k samples).

Bus Mastering DMA

The PCI/PCIe-7300A, cPCI-7300 performs high-speed data transfers between onboard FIFO and host memory using bus mastering DMA and scatter gather. When the PCI/PCIe-7300A, cPCI-7300 becomes the bus master, it takes control of the PCI/PCIe/cPCI bus, transfers data at burst speed, and then releases the bus. The host memory can be utilized as much as possible to store data when the data acquisition throughput is less than the sustained PCI bus bandwidth.

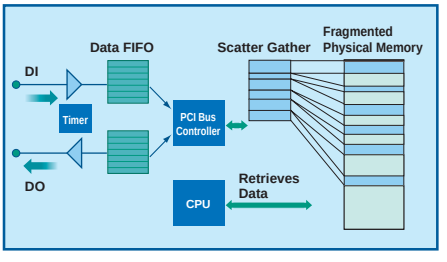
Scatter Gather Support

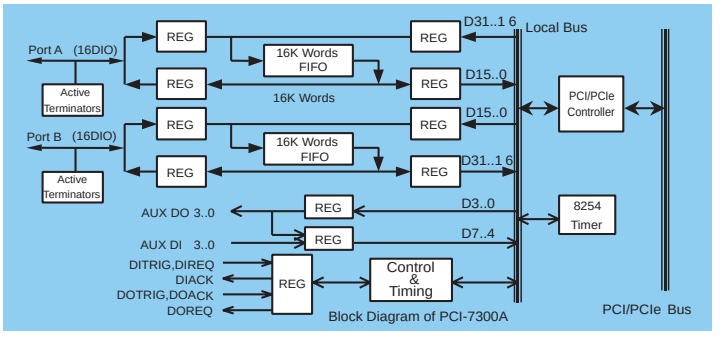
For bus master devices, the hardware has the special-design built-in support for transferring data to and from non-contiguous ranges of physical memory. The PCI/PCIe-7300A, cPCI-7300 contains multiple pairs of address and length registers, each one describing a single contiguous buffer segment. This allows the PCI/PCIe-7300A, cPCI-7300 to perform I/O using buffers that are scattered throughout DMA address space. These multiple address and count registers are often referred to as a scatter/gather list, and you can also think of these bus masters as having their own built-in mapping registers. With scatter gather support, the data transfer size is no longer a limitation, and moreover, ring buffer is easily achieved with the link list of the scattered memory.

I/O Port Configurations

The PCI/PCIe-7300A, cPCI-7300 is initially configured as two ports: PORT A and PORT B. Each port controls 16 digital I/O lines. The I/O ports can be configured as either input or output. According to outside device environment, the PCI/PCIe-7300A, cPCI-7300 can be configured to meet all high-speed digital I/O data transferring. PCI/PCIe-7300A, cPCI-7300 can support many different digital I/O operation modes:

- Internal clock: The digital input and output operations are handled by internal clock and data is transferred by busmastering DMA.
- External clock: The digital input and output operations are handled by external In/Out strobe signals (DI_REQ or DO_ACK) and data is transferred by busmastering DMA.
- Handshaking: Through REQ and ACK signals, the digital I/O data can have simple handshaking data transfer to guarantee no data loss.
- Pattern generation: The PCI/PCIe-7300A, cPCI-7300 reads or writes digital data at a prede termined rate. Users can control the rate internally via by onboard counters with 50 ns timing resolution.





Block Diagram of PCI-7300A

Features

- **x1 lane PCI Express® Interface (PCIe-7300A)**
- **Supports a 32-bit 5 V PCI bus (PCI-7300A)**
- **3U Eurocard form factor, CompactPCI compliant (PICMG 2.0 R2.1) (cPCI-7300)**
- **32-CH 5 V/TTL digital inputs/outputs**
- **20 MHz (80 MB/s) maximum transfer rate**
- **8, 16, or 32-bit transfers**
- **4 auxiliary DI & 4 auxiliary DO**
- **Onboard 64 kB FIFO**
- **Onboard programmable timer pacer clock**
- **Timed digital input sampling controlled by internal timer or external clock**
- **Independent trigger signals to start data acquisition and pattern generation**
- **Scatter-gather DMA**
- **Supports handshaking digital I/O transfer mode**
- **Repeated digital pattern generation from FIFO**
- **Active terminators for high-speed and longdistance data transfer**

Operating Systems

- Windows Vista/XP/2000/2003
- Linux

Recommended Software

- AD-Logger
- VB.NET/VC.NET/VB/VC++/BCB/Delphi
- DAQBench

Driver Support

- DAQPilot for Windows
- DAQPilot for LabVIEW™
- PCIS-DASK for Windows
- PCIS-DASK/X for Linux

Specifications

Digital I/O

- Numbers of channel (Software configurable)
  - 16 DI & 16 DO
  - 32 DI
  - 32 DO
- Compatibility: 5 V/TTL
- Digital logic levels
  - Input high voltage: 2-5.25 V
  - Input low voltage: 0-0.8 V
  - Output high voltage: 2.7 V minimum
  - Output low voltage: 0.5 V maximum
- Input load
  - Terminator OFF
    - Input high current: 1 mA
    - Input low current: 20 mA
  - Terminator ON
    - Termination resistor: 111 Ω
    - Termination voltage: 2.9 V
    - Input high current: 1 mA
    - Input low current: 22.4 mA
- Output driving capacity
  - Source current: 8 mA
  - Sink current: 48 mA

Transfer characteristics

- Data transfers:
  Bus-mastering DMA with Scatter/Gather
- Data width: 32/16/8 bits (programmable)

Data transfer count

- 2 M double words (8 MB) for non-chaining mode DMA
- No limitation for chaining mode (scatter/gather) DMA

Max transfer rate

- DO: 80 MBytes/s, 32-bit output @ 20 MHz
  DI: 80 MBytes/s, 32-bit input @ 20 MHz

Trigger

- DI_TRG for digital inputs,
  DO_TRG for digital outputs
- Compatibility: 5 V/TTL
- Trigger types: rising or falling edges
- Minimum pulse width: 32 ns

Clocking mode

- Internal clock
  - Internal clock sources: 20 MHz, 10 MHz, Timer#0 output (digital input pacer) and Timer #1 output (digital output pacer)
- External clock up to 40 MHz
- Handshaking
- Burst handshaking

Programmable counter

- Base clock: 10 MHz
- Timer #0 as digital input pacer
- Timer #1 as digital output pacer
- Timer #2: as interrupt source

Auxiliary digital I/O

- Number of channels
  - 4-CH digital inputs
  - 4-CH digital outputs
- Compatibility: 5 V/TTL
- Data transfers: programmed I/O

Auxiliary digital I/O

- I/O connector: 100-pin SCSI-II female
- Operating temperature: 0 °Cto 60°C
- Storage temperature: -20°C to 80°C
- Relative humidity: 5% to 95%, non-condensing
- Power requirements

Device	Power	Onboard terminator off	Onboard terminator on
PCI-7300A	+5 V	830 mA typical	1.0 A typicall
PCIe-7300A	+12 V	119 mA typical	287 mA typical
	+3.3 V	499 mA typical	543 mA typical
cPCI-7300	+5 V	830 mA typical	1.0 A typical

- Dimensions (not including connectors)
  - 179 mm x 106 mm (PCI-7300A)
  - 168 mm x 112 mm (PCIe-7300A)
  - 160 mm x 100 mm (cPCI-7300)

Terminal Boards

DIN-100S-01

Terminal Board with One 100-pin SCSI-II Connector and DIN-Rail Mounting (Cables are not included. For information on mating cables, refer to Section 12, Accessories.)

Note:
Legacy DIN-502S can be replaced by two DIN-50S-01 and ACL-10252-1 (100-Pin to two 50-Pin Cable, 1 M)

Ordering Information

PCI-7300A
80 MB/S High-Speed 32-CH Digital I/O Card

PCIe-7300A
80 MB/S High-Speed 32-CH Digital I/O PCIe Card

cPCI-7300
80 MB/s High-Speed 32-CH Digital I/O Module

Pin Assignment

GND	1	51	PB15
GND	2	52	PB14
GND	3	53	PB13
GND	4	54	PB12
GND	5	55	PB11
GND	6	56	PB10
GND	7	57	PB9
GND	8	58	PB8
GND	9	59	PB7
GND	10	60	PB6
GND	11	61	PB5
GND	12	62	PB4
GND	13	63	PB3
GND	14	64	PB2
GND	15	65	PB1
GND	16	66	PB0
GND	17	67	DO_ACK
GND	18	68	DO_REQ
GND	19	69	DO_TRG
GND	20	70	AUXO3
GND	21	71	AUXO2
GND	22	72	AUXO1
GND	23	73	AUXO0
GND	24	74	TERMPWR
GND	25	75	TERMPWR
GND	26	76	TERMPWR
GND	27	77	TERMPWR
GND	28	78	AUXI3
GND	29	79	AUXI2
GND	30	80	AUXI1
GND	31	81	AUXI0
GND	32	82	DI_ACK
GND	33	83	DI_REQ
GND	34	84	DI_TRG
GND	35	85	PA15
GND	36	86	PA14
GND	37	87	PA13
GND	38	88	PA12
GND	39	89	PA11
GND	40	90	PA10
GND	41	91	PA9
GND	42	92	PA8
GND	43	93	PA7
GND	44	94	PA6
GND	45	95	PA5
GND	46	96	PA4
GND	47	97	PA3
GND	48	98	PA2
GND	49	99	PA1
GND	50	100	PA0