For Technology
in Quality

# User's Manual

# STK52xx

**STK52xx UM 300**

**12.10.2010**

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# Revision history

| Rev. | Date | Name | Pos. | Modification |
|---|---|---|---|---|
| 005 | 10.08.2004 | ANW | | Created |
| 007 | 01.04.2005 | VJU | | Revised |
| 200 | 31.05.2005 | VJU | | Audio interface and RTC added |
| 201 | 10.08.2005 | VJU | | Revised according to test results |
| 300 | 12.10.2010 | F. Petz | | Completely revised |

# 1. About this Manual

This manual contains technical information concerning the Starterkit STK52xx.

## 1.1 Tips on Safety

Improper or incorrect handling of the product can substantially reduce its life span.

## 1.2 Terms and Conventions

| Symbol / Tag | Meaning |
|---|---|
|  | This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed with the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V. |
|  | This symbol indicates the possible use of voltages greater than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component. |
|  | This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used. |
|   | This symbol represents important details or aspects for working with TQ-products. |
| ***Filename.ext*** | This specification is used to state the complete file name with its corresponding extension. |
| `Instructions / Examples` | Examples of an application. e.g.,<br>• Specifying memory partitions<br>• Processing a script<br>• ..... |
| ***Reference*** | Cross-reference to another section, figure or table. |

Table 1: Terms and conventions

## 1.3 Handling and ESD tips

General handling of your TQ-products

| | |
|---|---|
|  | The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.<br><br>A general rule is: not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the system's power supply is switched off.<br><br>Violation of this guideline may result in damage / destruction of the module and be dangerous to your health.<br><br>Improper handling of your TQ-product renders the guarantee invalid. |

Proper ESD handling

| | |
|---|---|
|  | The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).<br><br>Always wear antistatic clothing and use ESD-safe tools, packing materials etc. and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices. |

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## 1.5 Imprint

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# 2. General

The STK52xx is a Starterkit, with which TQC Minimodule Type “TQM5200(S)” can be used.

The STK52xx Rev. 200 Starterkit has been developed for the subsequent requirements listed below.

1. Test and Development of MPC52xx based TQ-Minimodules like the TQM5200 and derivative products.
2. Description of the functions of TQ-Minimodule is based on MPC52xx (for presentations, measurements, etc.)
3. Development and test environment for realization and testing of additional function, which are not implemented on the TQ-Minimodules.
4. Standard product, for direct use by the customer.
5. The Starterkit provides all functions and interfaces of the TQ-Minimodule. Furthermore, additional functions like RTC, Sound and I/O functionality are available.

# 3. System Architecture

## 3.1 Block Diagram

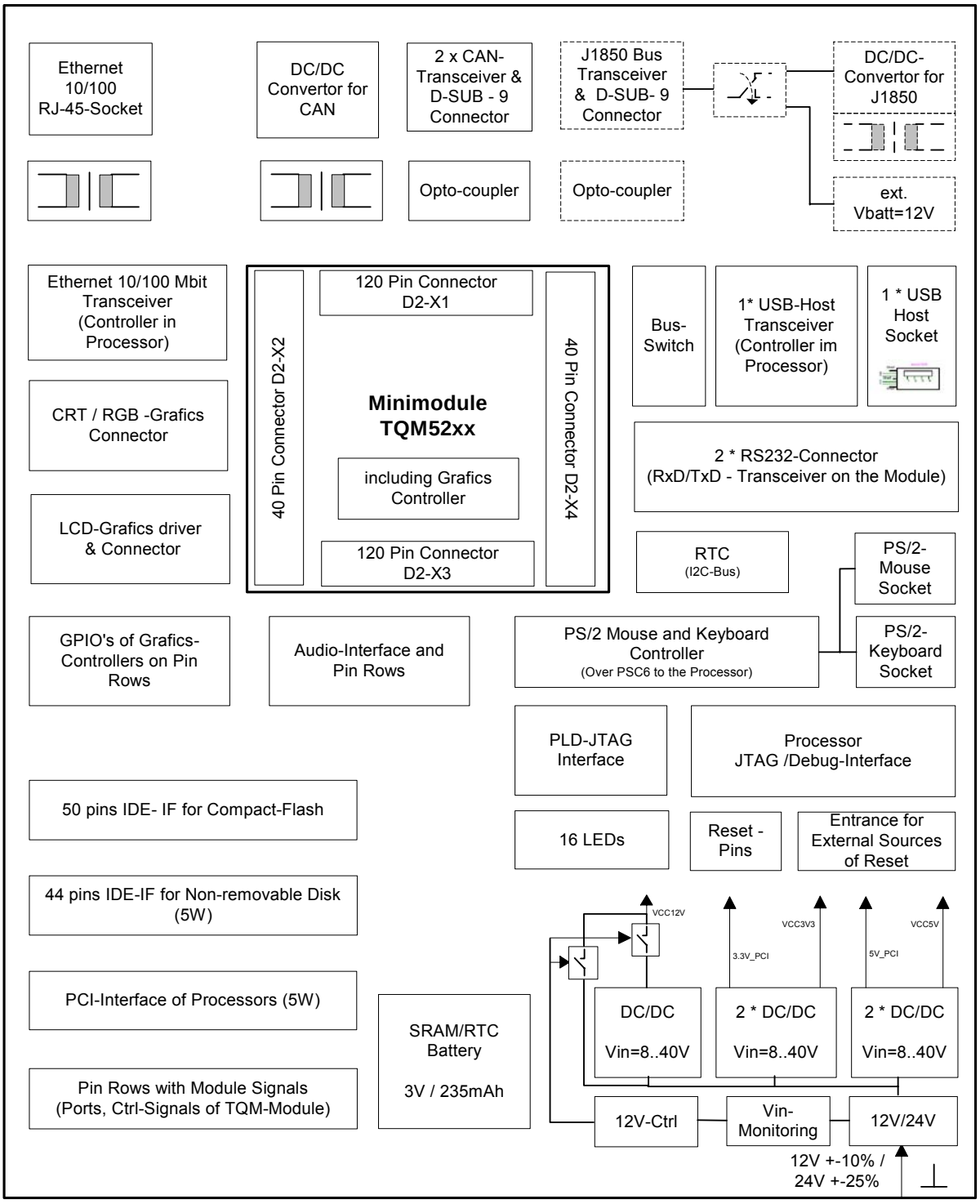


Illustration 1: STK52xx Rev. 200 Block Diagram

## 3.2 Functionality

- 1 × Ethernet interface with 10/100 Mbit transceiver
  - LXT971A
  - Controller in MPC52xx
- 2 × CAN interfaces (at I²C and timer-port)
  - PCA82C251
  - Galvanic isolation of the signals by optocouplers HCPL-060L and HCPL-0600
  - Galvanic isolation of power supply by DC/DC converters NTE0505
  - Controller in the MPC52xx
- 1 × J1850 bus with D-SUB-9 connector
  - AU5780A (Philips)
  - Galvanic isolated signals on optocouplers HCPL-0600 and HCPL-060L
  - Power supply on the external OBD-II-interface or galvanically separated 12 V
  - Controller in the MPC52xx
- 1 × USB 1.1 Host interface
  - USB1T11A with MIC2025 for power management, USB host socket
  - Controller in the MPC52xx
- 2 × RS232 interfaces (RxD, TxD, RTS and CTS)
  - TxD- and RxD transceiver on the module
  - RTS- and CTS transceiver on the Starterkit
- 1 × CRT – Graphics interface (only for modules with graphics controller)
  - Directly connected to the module
- 1 × LCD – Graphics interface (only for modules with graphics controller)
  - Connected to TQM5200 via LVC244A bus driver
- 1 × PS/2 keyboard and 1 × PS/2 mouse connector
  - PIC controller 16F627
  - Connected to TQM5200 via PSC6
- 1 × JTAG and debug interfaces for TQM5200 module (processor and PLD)
  - On pin strips with typical pin assignment
- 1 × Human interface (16 LEDs)
  - 16 red LEDs with drivers (8 × on the graphics controller, 4 × at the timer port, 4 × at PSC3)
- 1 × Module signal interface for all module pins
  - 320 pin interface (2 × 120 pins for processor signals, 2 × 40 pins for graphics signals)
- 1 × PCI interface (3.3 V)
  - 2 × 62-pin 32 bit standard PCI slot.
- 1 × IDE Master and Slave interface for Compact–Flash and fixed hard disk.
  - Standard 50-pins IDE interface (5 V), connected to ATA interface of MPC52xx on the TQM5200 for a Compact Flash
  - Standard 44-pins IDE interface (5 V) (2 mm pin strip) for the fixed hard disk. The Master / Slave switching takes place via jumper.
- 1 × Audio interface
  - PCM1772 stereo audio DAC
  - LM4867 dual 2.1 W audio amplifier
  - 4 pin strip on STK52xx (not bound outward)
- 1 × RTC (I²C) – timekeeper
- 1 × Back-up battery for RTC (Starterkit) and SRAM (Module, depending on versions)
  - Lithium battery 3 V / 235 mAh
- 1 × Reset button
- 1 × Power supply from an external standard mains adaptor (or power supply unit)
  - 12 V ±10 % or 24 V ±25 %

# 4. Electronics Specification

## 4.1 External Interfaces

In this section the interfaces of the STK52xx are described.

Generally on all signals, which are routed via connector, a discharger is implemented as an ESD preventive measure. Excepted from it are interfaces, which have ESD protection using the transceiver.

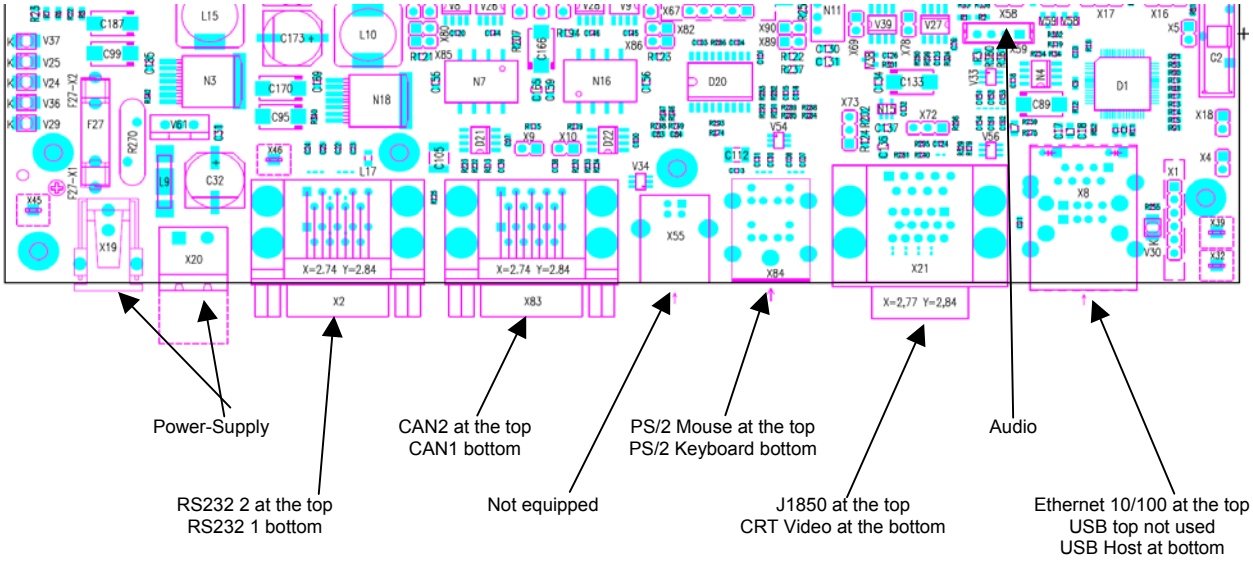


Illustration 2: Description of External Connectors

### 4.1.1 CRT Interface (X21)

Some TQM5200 modules are equipped with a graphics controller.

The CRT interface is routed to a standard D-SUB-15 connector.

| Pin | Signal | Type | Description |
|---|---|---|---|
| 1B | RED | O | ↓ 75 Ω |
| 2B | GREEN | O | ↓ 75 Ω |
| 3B | BLUE | O | ↓ 75 Ω |
| 4B | NC | - | Not Connected |
| 5B | DGND | - | Ground |
| 6B | DGND | - | Ground |
| 7B | DGND | - | Ground |
| 8B | DGND | - | Ground |
| 9B | VCC5VCRT | - | → Filter → Fuse (1 A) |
| 10B | DGND | - | Ground |
| 11B | NC | - | Not Connected |
| 12B | CRT_DDC_DATA | I/O | ↑ 4.7 kΩ → 22 Ω |
| 13B | CRT_HSYNC | O | → 22 Ω |
| 14B | CRT_VSYNC | O | → 22 Ω |
| 15B | CRT_DDC_CLK | I/O | ↑ 4.7 kΩ → 22 Ω |
| M1 | DGND | - | Ground |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 2: Pin Assignment of D-SUB-15 Connector (X21)

All signals are protected using diode circuits against VCC5V and DGND. ESD Cover module used: SRV05-4. As additional ESD protection dischargers are implemented in the signal and data lines.

### 4.1.2 LCD Interface (X41)

The LCD interface is used to connect an LCD or TFT monitor. All signals are fed via an octal bus buffer / bus driver 74LVC244A to the 44 pin strip connector X41.
Only modules with graphics controller support this interface.

| Pin | Signal | Description | 24 Bit | 18 Bit |
|---|---|---|---|---|
| 1 | DGND | Ground | | |
| 2 | B_FP_SHIFT | Shift clock | | |
| 3 | B_FP_LINE | HSYNC | | |
| 4 | B_FP_FRAME | VSYNC | | |
| 5 | DGND | Ground | | |
| 6 | B_FP_D18 | RED | R2 | R0 |

| Pin | Signal | Description | 24 Bit | 18 Bit |
|---|---|---|---|---|
| 7 | B_FP_D19 | RED | R3 | R1 |
| 8 | B_FP_D20 | RED | R4 | R2 |
| 9 | B_FP_D21 | RED | R5 | R3 |
| 10 | B_FP_D22 | RED | R6 | R4 |
| 11 | B_FP_D23 | RED | R7 | R5 |
| 12 | DGND | Ground | | |
| 13 | B_FP_D10 | GREEN | G2 | G0 |
| 14 | B_FP_D11 | GREEN | G3 | G1 |
| 15 | B_FP_D12 | GREEN | G4 | G2 |
| 16 | B_FP_D13 | GREEN | G5 | G3 |
| 17 | B_FP_D14 | GREEN | G6 | G4 |
| 18 | B_FP_D15 | GREEN | G7 | G5 |
| 19 | DGND | Ground | | |
| 20 | B_FP_D2 | BLUE | B2 | B0 |
| 21 | B_FP_D3 | BLUE | B3 | B1 |
| 22 | B_FP_D4 | BLUE | B4 | B2 |
| 23 | B_FP_D5 | BLUE | B5 | B3 |
| 24 | B_FP_D6 | BLUE | B6 | B4 |
| 25 | B_FP_D7 | BLUE | B7 | B5 |
| 26 | DGND | Ground | | |
| 27 | B_DRDY | READY | | |
| 28 | VCC3V3 | VCC3V3 | | |
| 29 | VCC3V3 | VCC3V3 | | |
| 30 | CNFHILO1 | Horizontal Select, NC, opt. ↑ or ↓ | | |
| 31 | CNFHILO2 | Vertical Select, NC, opt. ↑ or ↓ | | |
| 32 | VCC5V | VCC5V | | |
| 33 | B_FP_D16 | RED | R0 | |
| 34 | B_FP_D17 | RED | R1 | |
| 35 | DGND | Ground | | |
| 36 | B_FP_D8 | GREEN | G0 | |
| 37 | B_FP_D9 | GREEN | G1 | |
| 38 | DGND | Ground | | |
| 39 | B_FP_D0 | BLUE | B0 | |
| 40 | B_FP_D1 | BLUE | B1 | |
| 41 | DGND | Ground | | |
| 42 | VCC12V | VCC12V | | |
| 43 | VCC3V3 | VCC3V3 | | |
| 44 | B_FPEN | Power Down | | |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 3: Pin Assignment of TFT Connectors for the LCD Interface (X41)

To connect LVDS monitors / LVDS displays, the adapter ADAP-LVDS1 can be connected on the LCD interface (X41). For operation with DVI monitors, the ADAP-DVI device has to be connected to the LCD interface.

### 4.1.3 Extension Interface (X57)

The I²C signal data and clock of the graphics controller interface are fed to an extension connector. The extension interface can be used only for monitor identification while using ADAPDVI1 DVI adapter device.

| Pin | Signal | Type | Description |
|---|---|---|---|
| 1 | NC | | |
| 2 | NC | | |
| 3 | NC | | |
| 4 | GND | – | Ground |
| 5 | CRTDDCLK | I | I²C monitor detection clock |
| 6 | CRTDDCDATA | I/O | I²C monitor detection data |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 4: Pin Assignment of the Extension Interface (X57)

### 4.1.4 Backlight Supply (X7)

A second pin strip connector X7 is used to provide backlight supply for LCD or TFT monitor. Using a jumper (5VBCL), the internally generated +5V-supply or an external +5V-supply are selected. The 12 V backlight voltage is fused with 4 A; the 5 V with 3 A.

| Pin | Signal | Type | Description |
|---|---|---|---|
| 1 | VCC12V | – | Switched (MOSFET) VCC12V for backlight |
| 2 | VCC12V | – | Switched (MOSFET) VCC12V for backlight |
| 3 | DGND | – | Ground |
| 4 | DGND | – | Ground |
| 5 | VCC5V | – | Switched (MOSFET) VCC5V for backlight |
| 6 | VCC5V | – | Switched (MOSFET) VCC5V for backlight |

Table 5: Pin Assignment of the Backlight Connectors (X7)

### 4.1.5 Keyboard and Mouse Controller (X84)

A keyboard and mouse controller is used as the input device, which communicates with the TQM5200 via the serial interface of the PSC6 (Programmable Serial Controller, UART 6).

SRV05-4 is used for both the PS2 interfaces as ESD protection.

A colour coded, stacked PS/2 socked (X84) is used.

#### 4.1.5.1 Mouse X84 (top, green)

| Pin | Signal | Type | Description |
|---|---|---|---|
| B1 | MSDATA | I/O | ↑4.7 kΩ, ↓100 pF |
| B2 | NC | – | Not connected |
| B3 | DGND | – | Ground |
| B5 | VCC5V ON | – | Connected to pin A5 |
| B6 | MSCLK | I/O | ↑4.7 kΩ, ↓100 pF |
| B8 | NC | – | Not connected |
| M1 | DGND | – | Ground |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 6: Pin Assignment of Mouse Connector (X84)

#### 4.1.5.2 Keyboard X84 (bottom, purple)

| Pin | Signal | Type | Description |
|---|---|---|---|
| A1 | KBDATA | I/O | ↑4.7 kΩ, ↓100 pF |
| A2 | NC | – | Not connected |
| A3 | DGND | – | Ground |
| A5 | VCC5V ON | – | VCC5V; ↓100 nF\|\|10 µF, → fuse (0.5 A) → ferrite bead |
| A6 | KBCLK | I/O | ↑4.7 kΩ, ↓100 pF |
| A8 | NC | – | Not connected |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 7: Pin Assignment of Keyboard Connector (X84)

### 4.1.6 Programming Interface for Keyboard and Mouse Controller (X67)

The software of keyboard controller is downloaded via Microchip Download interface from the PIC16F627 in the on-chip program memory.

| Pin Number | Description |
|---|---|
| 1 | RB6/T1OSO/T1CKI |
| 2 | RB7/T1OSI |
| 3 | DGND |
| 4 | VCC5V |
| 5 | RA5/#MCLR/THV |

Table 8: Pin Assignment of the Programming Interface of PIC16F627 (X67)

### 4.1.7 Audio Interface (X59)

For sound, an audio DAC is connected to the module connector at I2S Port/CODEC Port (PSC2.0 – PSC2.4).

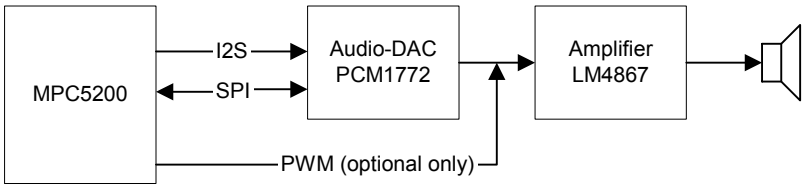


Illustration 3: Audio

The SPI interface (PSC3.6 – PSC3.9) is required for the configuration of the DAC register.

The PCM1772 of Texas Instruments is used as audio DAC. It offers the following features:

- Audio DAC stereo
- 24 bit resolution
- I2S and 16 bit word; right aligned
- Lineout amplifier + internal gain control (controlled over SPI)

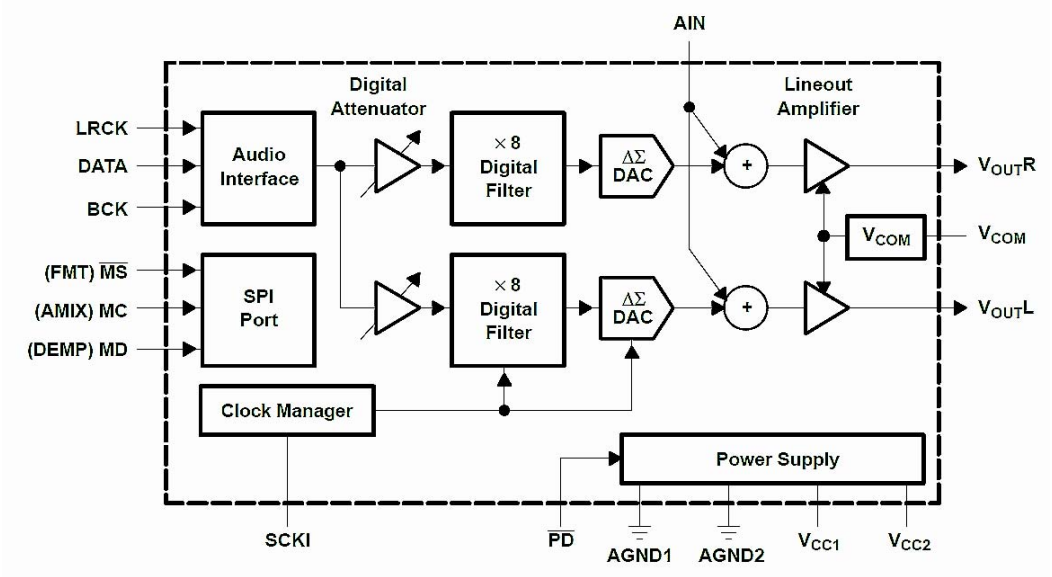


Illustration 4: Audio DAC Block Diagram

The AIN pin can be accessed via the Timer2 pin of the module (Timer port bit 2).
The Timer2 pin is connected via a low pass filter and a serial capacitor (1 µF) to AIN.

As audio amplifier, the LM4867 of National Semiconductor is used.
This amplifier offers an output power of up to 1.9 W. (5 V supply; 4 Ω, output load.)

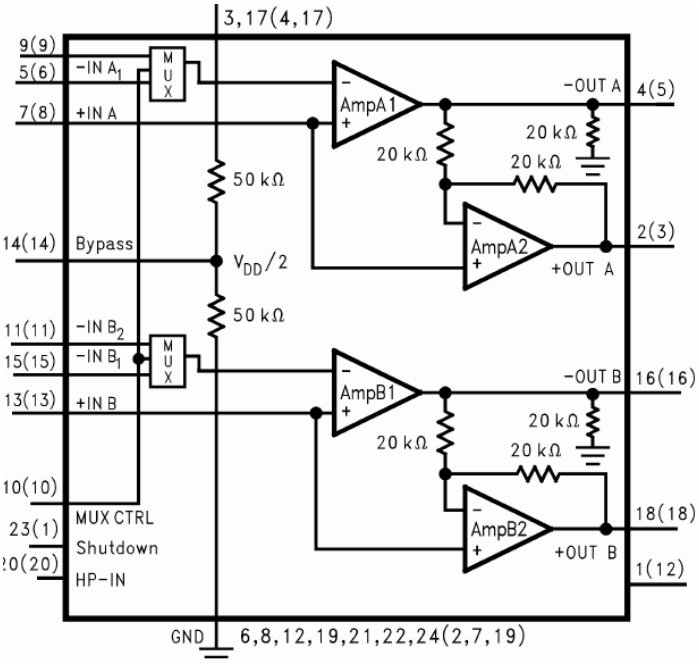


Illustration 5: Audio Amplifier Block Diagram

An LC Filter in the power supply serves to reduce noise.

| Pin | Signal | Type | Description |
|---|---|---|---|
| 1 | OutA- | O | Audio_out1 |
| 2 | OutA+ | O | Audio_out1 |
| 3 | OutB- | O | Audio_out2 |
| 4 | OutB+ | O | Audio_out2 |

Table 9: Pin Assignment of 4-Pin Connector (X59)

The sound interface is not fed on a connector to the device front and is not provided with an ESD protective circuit.

### 4.1.8 10/100 Mbit Ethernet Interface (X8)

A 10/100 Mbit Ethernet interface is available to connect to a network. For this purpose, a +3.3 V Dual Speed Fast Ethernet PHY Transceiver (Intel LXT971A) is used with RJ45 socket with integrated transformer (Pulse JU054P01R/Dual USB/10/100 Mbit RJ45 Ethernet socket and transformer).

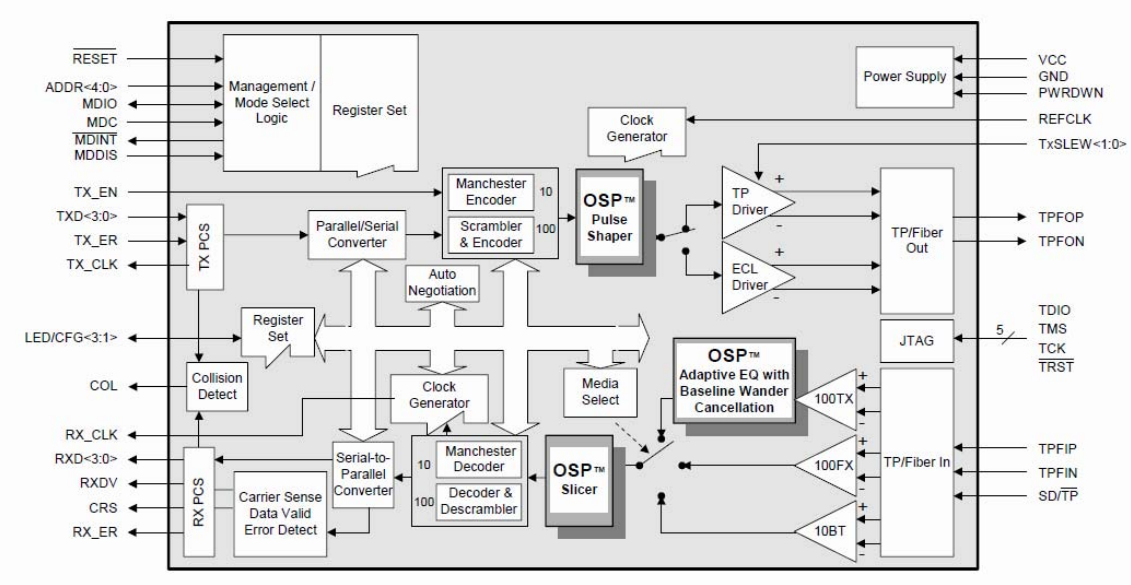


Illustration 6: LTX971 Block Diagram

The RJ45 jack includes integrated LEDs (yellow, green) and is completely shielded.
The transceiver module is connected to the TQM5200 module via the Ethernet interface.
Interrupt IRQ2 of the MPC52xx (enabled via jumper X13) is used for the Ethernet interrupt.

Jumpers are available on the Starterkit to set various modes of the LXT971A.

- X13 ⇨ Modes
- X18 ⇨ Pause
- X5 ⇨ PWRDWN
- X4 ⇨ Sleep
- X16 ⇨ TXSLEW1
- X17 ⇨ TXSLEW0

| Pin | Signal | Type | Description |
|---|---|---|---|
| 1 | TX+ | O | Galvanically decoupled |
| 2 | TX- | O | Galvanically decoupled |
| 3 | RX+ | I | Galvanically decoupled |
| 4 | Term plane | – | → 75 Ω, AC coupling to ground |
| 5 | Term plane | – | → 75 Ω, AC coupling to ground |
| 6 | RX- | I | Galvanically decoupled |
| 7 | Term plane | – | → 75 Ω, AC coupling to ground |
| 8 | Term plane | – | → 75 Ω, AC coupling to ground |
| M1 | DGND | – | Ground |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 10: Pin Assignment of RJ45 Socket (X8)

### 4.1.9 JTAG Interface to Ethernet PHY (X1)

The transceiver LXT971A can be configured using a JTAG interface (X1).

| Pin | JTAG Interface LXT971A |
|---|---|
| 1 | TDI |
| 2 | TDO |
| 3 | TMS |
| 4 | TCK |
| 5 | /TRST |
| 6 | GND |

Table 11: Pin Assignment of JTAG Interface (X1)

### 4.1.10 USB Host Interface (X8U)

The USB1 Host interface of the MPC52xx is connected using the USB transceiver USB1T11A.

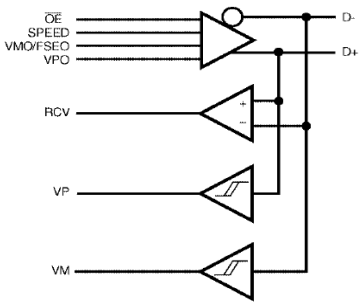


Illustration 7: USB1T11A Logic Diagram

For decoupling FET switches SN74CBTLV3384 are used. For the power management of the USB interface, a MIC2025 is used, which delivers power from its +5 V supply to the USB bus directly, which is available for external devices.

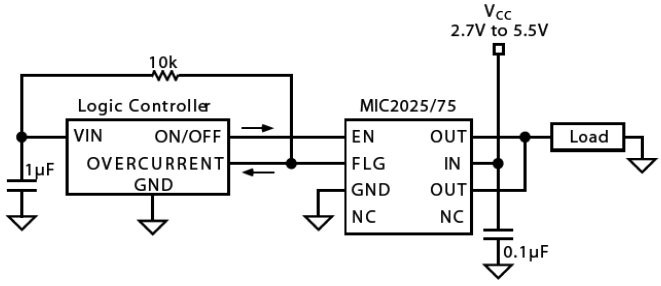


Illustration 8: Protective Circuit of MIC2025

The USB interface is USB1.1 compatible. The transfer rate conforms to the Low speed and the Full speed Specification. With USB 2.0-Devices, Full speed data rate can be achieved.

| Pin | Signal | Type | Description |
|---|---|---|---|
| L | DGND | – | Ground |
| U1_1 | VCC5V | – | VCC5V behind current limiter 0.5 A, ↓ 47 µF |
| U1_2 | USB- | I/O | From USB1T11A |
| U1_3 | USB+ | I/O | From USB1T11A |
| U1_4 | DGND | – | Ground |
| U2_1 | VCC5V | – | NC |
| U2_2 | P1- | I/O | NC |
| U2_3 | P1+ | I/O | NC |
| U2_4 | DGND | – | NC |
| R | DGND | – | Ground |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 12: Pin Assignment USB HOST Connector (X8 bottom)

As additional ESD protection, an array of diodes type SRV05-4 has been added to the signal lines.

| | |
|---|---|
| ! note ! | In the Starterkit a connector with dual USB-Host socket and RJ45 Ethernet socket is provided. Only the lower USB socket is connected. The upper USB socket is not implemented thus cannot be used. |

### 4.1.11 CAN Interface (X83)

Two CAN interfaces are implemented via the MSCAN interface of the MPC52xx.

Every CAN interface conforms to CAN Standard according to ISO11898 (CAN 2.0A, CAN2.0B).

The interfaces of MSCAN controller can be routed to different processor pins of the MPC5200, which are connected on the TQM5200 module to the module pins.
For STK52xx, the following configuration is specified:

- CAN1_TX: I²C_0 optionally at PSC2_0 configurable using 0 Ω resistors (option)
- CAN1_RX: I²C_1 optionally at PSC2_1 configurable using 0 Ω resistors (option)
- CAN2_TX: Timer_0, optionally at PSC2_2 configurable using 0 Ω resistors (option)
- CAN2_RX: Timer_1, optionally at PSC2_3 configurable using 0 Ω resistors (option)
- PSC2_4: WAKE_UP function

The outputs of MSCAN Controller are connected using CAN transceiver driver PCA82C251. This interface connection is provided with a galvanic isolation. For the implementation of the galvanic isolation of the signals optocouplers HCPL-060L and HCPL-0600 are used, which also work as a level shifter.

The supply voltage of both modules is +5 V. The supply of the CAN transceiver is galvanically isolated. For galvanic isolation a DC/DC converter NTE0505 is used.

Both CAN interfaces are independent of each other and galvanically isolated. For galvanic isolation, the following data applies:

- 1 kV, 3.9 mm

Moreover, the operation mode, High Speed or Silent of the transceiver can be set using jumpers (X9, X10). The default setting (jumper open) is the High Speed mode. In the Silent mode, the transceiver only listens on the bus and the transmitter is disabled.

A 9-pin double jack D-SUB connector is used for the CAN transceiver. Additionally, the bus termination is provided with 120 Ω, which is not included at the time of delivery. The maximum possible data rate is 1 Mbaud. The data transmission speeds are dependent on the line length, line type used and the number of the bus sharing units. The transfer rates stated below result from the sample test structure of a CAN Network composed of 2 bus sharing units and the line type LAPP 2170204T.

- Max. 600 kbaud with line length ≤ 100 m
  Max. 1 Mbaud with line length ≤ 25 m

| Pin Number | CAN1.2 Connector (D-SUB 9-pin) | Description |
|---|---|---|
| 1A / 1B | N.C. | – |
| 2A / 2B | CANL | Data signal – |
| 3A / 3B | GND_CAN | Galvanically separated CAN ground |
| 4A / 4B | N.C. | – |
| 5A / 5B | N.C. | – |
| 6A / 6B | GND_CAN1 | Galvanically separated CAN ground |
| 7A / 7B | CANH | Data signal + |
| 8A / 8B | N.C. | – |
| 9A / 9B | +5 V | Galvanically separated CAN supply |

Table 13: Pin Assignment CAN Interface (X83)

The CAN interfaces are not provided with additional ESD protective circuitry.

### 4.1.12 J1850–Bus (X21)

The MPC52xx supports the bus system as per SAE/J1850 VPW, which is widely used in the USA and whose use is also widespread in the automobile industry. That is why a J1850 interface is provided optionally via an OBD-II cable interface with the Starterkit.

A Philips AU5780A is used as the J1850 transceiver. It is powered via the OBD-II connection. Both digital signals TX and RX are connected via two optocouplers HPCL-0600 to the MPC52xx to achieve galvanic isolation. The optocouplers also take over the function of level shifting. For galvanic isolation the following data applies:

- 1 kV, 3.9 mm
- The J1850 interface of the MPC52xx is located in the Ethernet port group. These pins are used:
  - Pin ETH_4 (J02) through J1850_TX
  - Pin ETH_13 (M01) through J1850_RX

| | |
|---|---|
| ! note ! | The use of the J1850 interface causes constraints with respect to the Ethernet interface. With this, only the 10 Mbps 7-wire interface can be used.<br>**The use of the 10/100 Mbps 18-wire interface implemented on the STK52xx is not possible simultaneously with the J1850 interface.**<br>Three 3-pin jumpers are necessary for the switchover (X64, X74, X76), two for the signal path of the pins ETH_4 and ETH_13 and one for a GPIO input for the display of the mode set by the user. The setting of the operation mode must be done when the unit is powered off, so that the software, at the time of switching on, can read the setting during its initialization phase. |

For mode setting pin PSC3_8 (A05) as INIT_ETH/J1850_MODE is used.

The function modules of the PSC3 group can be used only to a limited extent owing to the allocation of PSC3_0 to PSC3_7 with LEDs. That is why the mode setting is the least of problems here. The jumper signal is connected via a 10 kΩ resistor with PSC3_8. Thus, the port pin is freely available as an output port after the initialization, and is also available conditionally as an input port (owing to the undefined status “0“ or “1“ via the 10 kΩ resistor).

The power supply to the AU5780A transceiver module is fed either by battery or a galvanic isolated voltage of +12 V (max. 24 V). During operation, the current consumption is approx. 10 mA, and, in case of a short circuit at the bus, max. 60 mA. The SAE/J1850 VPW bus line works with a level of approx. 8 V. The NME1212 with 1 W, approx. 80 mA, and galvanic isolated DC/DC converter is used.

The AU5780A module works without Supply Control Function.

On the Starterkit a 9-pin D-SUB connector is used for connection of a standard OBD-II cable.

When using an OBD-II cable an external adapter must be connected (not a standard accessory of the STK52xx Starterkit).

The pin assignment of the J1850 controller on the D-SUB-9 connector (X21) matches the standard assignment as per OBDIIJ1962.

| D-SUB 9-pin (Male Connector on STK52xx) | J1962-Signal description | Notes for the Starterkit |
|---|---|---|
| 1 | Signal GND | N.C. (Because of galvanic isolation) |
| 2 | Chassis GND | N.C. |
| 3 | CANH (J-2284) | N.C. |
| 4 | ISO9141-2 K – Line | N.C. |
| 5 | CANL (J-2284) | N.C. |
| 6 | J1850-bus (-) | BUS Ground (AGND) |
| 7 | J1850-bus (+) | BUS Line |
| 8 | ISO9141-2 L – Line | N.C. |
| 9 | Battery Power | +12 V (via OBD-II cable) |

Table 14: Pin Assignment of the J1850 Controller

### 4.1.13 2 × RS232 Interface (X2)

Two serial interfaces are available on the Starterkit, and both are made available externally on the Starterkit by means of standard RS232 connectors (D-SUB 9-pin).

The transfer rate is 9.6 kbaud up to 115.2 kbaud (line length ≤5 m, line type Belden 9829 060500). The transmission rates depend on the length of line, the number of bus subscribers, the quality of the line used and the type of scheduling.

| Pin | Signal | Type | Description |
|---|---|---|---|
| 1A / 1B | NC | – | |
| 2A / 2B | RXD | I | From RS232 transceiver (Module) |
| 3A / 3B | TXD | O | From RS232 transceiver (Module) |
| 4A / 4B | NC | – | |
| 5A / 5B | DGND | – | Ground |
| 6A / 6B | NC | – | |
| 7A / 7B | RTS# | O | From RS232 transceiver (STK52xx) |
| 8A / 8B | CTS# | I | From RS232 transceiver (STK52xx) |
| 9A / 9B | N.C. | – | |
| M1 | DGND | – | Ground |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 15: Pin Assignment (X2)

Additional protection is provided on the signal lines to protect from Electrostatic discharge (ESD).

The bus drivers for RxD and TxD are assembled on the module, the drivers for RTS and CTS are assembled on the Starterkit.

### 4.1.14 PCI Slot (X47)

The internal PCI 2.2 compatible interface of the MPC52xx is made available on the Starterkit to a PCI slot.

The PCI controller of the MPC5200 supports type-0 configurations and can work as master as well as in slave-mode. The arbiter directly addresses an external slave and always supplies the PCI clock for the PCI bus.

| | |
|---|---|
| ! note ! | The MPC52xx is not 5V-tolerant at the PCI interface.<br>Thus, only 3.3 V PCI devices can be connected! |

| Pin | Signal | Type | Description |
|---|---|---|---|
| X4_A1 | TRST# | I/O | NC |
| X4_A2 | VCC12V | – | VCC12V |
| X4_A3 | TMS | I/O | ↑ 5.6 kΩ to VCC3.3V; optional VCC5V |
| X4_A4 | TDI | I/O | ↑ 5.6 kΩ to VCC3.3V; optional VCC5V |
| X4_A5 | VCC5V | – | VCC5V |
| X4_A6 | INTA# | I | ↑ 5.6 kΩ to VCC3.3V; IRQ0; direct from TQM5200(S) |
| X4_A7 | INTC# | I | ↑ 5.6 kΩ to VCC3.3V |
| X4_A8 | VCC5V | – | VCC5V |
| X4_A9 | NC | I/O | NC |
| X4_A10 | VCC5V | – | VCC3.3V |
| X4_A11 | NC | I/O | NC |
| X4_A12 | DGND | – | Ground |
| X4_A13 | DGND | – | Ground |
| X4_A14 | 3V3AUX | – | VCC3.3V |
| X4_A15 | PCIRST# | I/O | #PCI_RESET; direct from TQM5200(S) |
| X4_A16 | VCCIO | – | VCC3.3V; optional VCC5V |
| X4_A17 | GNT0# | I/O | #PCI_GNT; direct from TQM5200(S) |
| X4_A18 | DGND | – | Ground |
| X4_A19 | NC | I/O | NC |
| X4_A20 | AD30 | I/O | Direct from TQM5200(S) |
| X4_A21 | VCC3V3 | – | VCC3V3 |
| X4_A22 | AD28 | I/O | Direct from TQM5200(S) |
| X4_A23 | AD26 | I/O | Direct from TQM5200(S) |
| X4_A24 | DGND | – | Ground |
| X4_A25 | AD24 | I/O | Direct from TQM5200(S) |
| X4_A26 | IDSEL1 | I/O | Direct from TQM5200(S) |
| X4_A27 | VCC3V3 | – | VCC3V3 |

| Pin | Signal | Type | Description |
|---|---|---|---|
| X4_A28 | AD22 | I/O | Direct from TQM5200(S) |
| X4_A29 | AD20 | I/O | Direct from TQM5200(S) |
| X4_A30 | DGND | – | Ground |
| X4_A31 | AD18 | I/O | Direct from TQM5200(S) |
| X4_A32 | AD16 | I/O | Direct from TQM5200(S) |
| X4_A33 | VCC3V3 | – | VCC3V3 |
| X4_A34 | FRAME# | I/O | #PCI_FRAME; direct from TQM5200(S) |
| X4_A35 | DGND | – | Ground |
| X4_A36 | TRDY# | I/O | #PCI_TRDY; direct from TQM5200(S) |
| X4_A37 | DGND | – | Ground |
| X4_A38 | STOP# | I/O | #PCI_STOP; direct from TQM5200(S) |
| X4_A39 | VCC3V3 | – | VCC3V3 |
| X4_A40 | SDONE | I/O | ↑ 5.6 kΩ to VCC3.3V; optional VCC5V |
| X4_A41 | SB0# | I/O | ↑ 5.6 kΩ to VCC3.3V; optional VCC5V |
| X4_A42 | DGND | – | Ground |
| X4_A43 | PAR | I/O | PCI_PAR; direct from TQM5200(S) |
| X4_A44 | AD15 | I/O | Direct from TQM5200(S) |
| X4_A45 | VCC3V3 | – | VCC3V3 |
| X4_A46 | AD13 | I/O | Direct from TQM5200(S) |
| X4_A47 | AD11 | I/O | Direct from TQM5200(S) |
| X4_A48 | DGND | – | Ground |
| X4_A49 | AD9 | I/O | Direct from TQM5200(S) |
| X4_A50 | DGND | – | Ground; NC –GAP |
| X4_A50 | DGND | – | Ground; NC –GAP |
| X4_A52 | C/BE0# | I/O | PCI_CBIO; direct from TQM5200(S) |
| X4_A53 | VCC3V3 | – | VCC3V3 |
| X4_A54 | AD6 | I/O | Direct from TQM5200(S) |
| X4_A55 | AD4 | I/O | Direct from TQM5200(S) |
| X4_A56 | DGND | – | Ground |
| X4_A57 | AD2 | I/O | Direct from TQM5200(S) |
| X4_A58 | AD0 | I/O | Direct from TQM5200(S) |
| X4_A59 | VCCIO | – | VCC3.3V; optional VCC5V |
| X4_A60 | REQ64# | I/O | ↑ 5.6 kΩ to VCC3.3V; optional VCC5V |
| X4_A61 | VCC5V | – | VCC5V |
| X4_A62 | VCC5V | – | VCC5V |
| | | | |
| X4_B1 | VSS-12V | – | NC |
| X4_B2 | TCK | I/O | NC |
| X4_B3 | DGND | – | Ground |

| Pin | Signal | Type | Description |
|---|---|---|---|
| X4_B4 | TDO | I/O | NC |
| X4_B5 | VCC5V | – | VCC5V |
| X4_B6 | VCC5V | – | VCC5V |
| X4_B7 | INTB# | I | ↑ 5.6 kΩ to VCC3.3V; NC |
| X4_B8 | INTD# | I | ↑ 5.6 kΩ to VCC3.3V; NC |
| X4_B9 | PRSNT1 | I/O | NC |
| X4_B10 | NC | I/O | NC |
| X4_B11 | PRSNT2 | I/O | NC |
| X4_B12 | DGND | – | Ground |
| X4_B13 | DGND | – | Ground |
| X4_B14 | NC | I/O | NC |
| X4_B15 | DGND | – | Ground |
| X4_B16 | PCI_CLK0 | O | PCI_CLK; direct from TQM5200(S) |
| X4_B17 | DGND | – | Ground |
| X4_B18 | REQ0# | I/O | #PCI_REQ; direct from TQM5200(S) |
| X4_B19 | VCCIO | – | VCC3V3V optional 5V |
| X4_B20 | AD31 | I/O | Direct from TQM5200(S) |
| X4_B21 | AD29 | I/O | Direct from TQM5200(S) |
| X4_B22 | DGND | – | Ground |
| X4_B23 | AD27 | I/O | Direct from TQM5200(S) |
| X4_B24 | AD25 | I/O | Direct from TQM5200(S) |
| X4_B25 | VCC3V3 | – | VCC3V3 |
| X4_B26 | C/BE3# | I/O | #PCI_CBE3; direct from TQM5200(S) |
| X4_B27 | AD23 | I/O | Direct from TQM5200(S) |
| X4_B28 | DGND | – | Ground |
| X4_B29 | AD21 | I/O | Direct from TQM5200(S) |
| X4_B30 | AD19 | I/O | Direct from TQM5200(S) |
| X4_B31 | VCC3V3 | – | VCC3V3 |
| X4_B32 | AD17 | I/O | Direct from TQM5200(S) |
| X4_B33 | C/BE2# | I/O | #PCI_CBE2; direct from TQM5200(S) |
| X4_B34 | DGND | – | Ground |
| X4_B35 | IRDY# | I/O | #PCI_IRDY; direct from TQM5200(S) |
| X4_B36 | VCC3V3 | – | VCC3V3 |
| X4_B37 | DEVSEL# | I/O | #PCI_DEVSEL; ↑ 5.6 kΩ VCC3.3V; direct from TQM5200(S) |
| X4_B38 | DGND | – | Ground |
| X4_B39 | LOCK# | I/O | ↑ 5.6 kΩ to VCC3.3V; NC |
| X4_B40 | PERR# | O | #PCI_PERR; direct from TQM5200(S) |
| X4_B41 | VCC3V3 | – | VCC3V3 |

| Pin | Signal | Type | Description |
|---|---|---|---|
| X4_B42 | SERR# | O | #PCI_SERR; direct from TQM5200(S) |
| X4_B43 | VCC3V3 | – | VCC3V3 |
| X4_B44 | C/BE1# | I/O | #PCI_CBE1; direct from TQM5200(S) |
| X4_B45 | AD14 | I/O | Direct from TQM5200(S) |
| X4_B46 | DGND | – | Ground |
| X4_B47 | AD12 | I/O | Direct from TQM5200(S) |
| X4_B48 | AD10 | I/O | Direct from TQM5200(S) |
| X4_B49 | M66EN | – | ↓ 10 nF; ↑ 3.3 kΩ VCC3.3V; M66EN (DGND-jumper X52) (1 = 66 MHz, 0 = 33 MHz) |
| X4_B50 | DGND | – | Ground; NC –GAP |
| X4_B51 | DGND | – | Ground; NC –GAP |
| X4_B52 | AD8 | I/O | Direct from TQM5200(S) |
| X4_B53 | AD7 | I/O | Direct from TQM5200(S) |
| X4_B54 | VCC3V3 | – | VCC3V3 |
| X4_B55 | AD5 | I/O | Direct from TQM5200(S) |
| X4_B56 | AD3 | I/O | Direct from TQM5200(S) |
| X4_B57 | DGND | – | Ground |
| X4_B58 | AD1 | I/O | Direct from TQM5200(S) |
| X4_B59 | VCCIO | – | VCC3.3V; optional VCC5V |
| X4_B60 | ACK64# | I/O | VCC3.3V; optional VCC5V |
| X4_B61 | VCC5V | – | VCC5V |
| X4_B62 | VCC5V | – | VCC5V |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 16: Pin Assignment PCI Interface (X47)

The signals of the PCI bus are fed without level shifter and / or buffer/driver directly to the TQM5200 module.

### 4.1.15 IDE Interface for Compact Flash and Hard Disk

An IDE and / or ATA interface is available on the STK52xx. The bus interface on the STK52xx is provided via standard IDE and / or ATA connectors. Since the ATA bus works with +5 V, level shifters are used for the bus signals.

#### 4.1.15.1 IDE Interface for Hard Disk(X48)

| Pin-No. | Signal | Type | Description |
|---|---|---|---|
| 1 | /ATA_RES | O | /ATA_RES from module (HW-Reset or SW-Reset (PSC1.4)) → 22 Ω; 5 V |
| 2 | DGND | – | DGND |
| 3 | DD7 | I/O | ↓10 kΩ, → 22 Ω; 5 V |
| 4 | DD8 | I/O | → 22 Ω; 5 V |
| 5 | DD6 | I/O | → 22 Ω; 5 V |
| 6 | DD9 | I/O | → 22 Ω; 5 V |
| 7 | DD5 | I/O | → 22 Ω; 5 V |
| 8 | DD10 | I/O | → 22 Ω; 5 V |
| 9 | DD4 | I/O | → 22 Ω; 5 V |
| 10 | DD11 | I/O | → 22 Ω; 5 V |
| 11 | DD3 | I/O | → 22 Ω; 5 V |
| 12 | DD12 | I/O | → 22 Ω; 5 V |
| 13 | DD2 | I/O | → 22 Ω; 5 V |
| 14 | DD13 | I/O | → 22 Ω; 5 V |
| 15 | DD1 | I/O | → 22 Ω; 5 V |
| 16 | DD14 | I/O | → 22 Ω; 5 V |
| 17 | DD0 | I/O | → 22 Ω; 5 V |
| 18 | DD15 | I/O | → 22 Ω; 5 V |
| 19 | DGND | – | DND |
| 20 | N.C. | – | NC |
| 21 | ATA_DMARQ | I | → 82 Ω; 5 V, ↓10 kΩ |
| 22 | DGND | – | DGND |
| 23 | IOWR# | O | ATA_IOWR#, → 22 Ω; 5 V |
| 24 | DGND | – | DGND |
| 25 | IOR# | O | ATA_IOR#; → 22 Ω; 5 V, ↑10 kΩ |
| 26 | DGND | – | DGND |
| 27 | IOCHRDY | I | ATA_ IOCHRDY, → 82 Ω; 5 V, ↑1 kΩ |
| 28 | Cable Select | – | Jumper X68 (1-2 = Slave ↑10 kΩ, 2-3 = Master ↓330 Ω) |
| 29 | DACK# | O | ATA_DMACK#, → 22 Ω; 5 V |
| 30 | DGND | – | DGND |
| 31 | ATA_INTRQ1 | I | ATA_INTRQ1, → 22 Ω; 5 V, ↓10 kΩ |
| 32 | IOCS16# | – | → 22 Ω; 5 V, ↑1 kΩ, 0 Ω to the module not assembled |
| 33 | DA1 | O | ATA_ADR1 (from A17) → 22 Ω; 5 V |
| 34 | CBLIDFP# | I/(O) | ↓ 100 kΩ GND, ↓ 47 nF GND, → 0 Ω, optional PSC3.3 |
| 35 | DA0 | O | ATA_ADR0 (from A16) → 22 Ω; 5 V |

| Pin-No. | Signal | Type | Description |
|---|---|---|---|
| 36 | DA2 | O | ATA_ADR2 (from A18) → 22 Ω; 5 V |
| 37 | CS0# | O | ATA_CS0# (from LP_CS4#) → 22 Ω; 5 V |
| 38 | CS1# | O | ATA_CS1# (from LP_CS5#) → 22 Ω; 5 V |
| 39 | HDDACT | I | Input for HDD activity → 22 Ω; 5 V, optional PSC3.1 |
| 40 | DGND | – | DGND |
| 41 | VCC5V_FP | – | VCC5V |
| 42 | VCC5V_FP | – | VCC5V |
| 43 | DGND | – | DGND |
| 44 | N.C. | – | NC |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 17: Pin Assignment IDE Interface (X48)

The I/O – type shown in the pin assignment is to be considered from the point of view of the TQM5200 module.

Primary Master or Slave can be selected with jumper (X68).

#### 4.1.15.2 IDE Interface for Compact Flash (X50)

| Pin No. | Signal | Type | Description |
|---|---|---|---|
| 1 | DGND | – | DGND |
| 2 | DD3 | I/O | → 33 Ω; 5 V |
| 3 | DD4 | I/O | → 33 Ω; 5 V |
| 4 | DD5 | I/O | → 33 Ω; 5 V |
| 5 | DD6 | I/O | → 33 Ω; 5 V |
| 6 | DD7 | I/O | → 33 Ω; 5 V |
| 7 | CS0# | O | ATA_CS0# (on LP_CS4#); → 22 Ω; 5 V |
| 8 | DGND | – | DGND |
| 9 | DGND | – | DGND |
| 10 | DGND | – | DGND |
| 11 | DGND | – | DGND |
| 12 | DGND | – | DGND |
| 13 | VCC5V | – | VCC5V |
| 14 | DGND | – | DGND |
| 15 | DGND | – | DGND |
| 16 | DGND | – | DGND |
| 17 | DGND | – | DGND |

| Pin No. | Signal | Type | Description |
|---|---|---|---|
| 18 | AD2 | O | ATA_ADR2 (on A18); → 22 Ω; 5 V |
| 19 | AD1 | O | ATA_ADR1 (on A17); → 22 Ω; 5 V |
| 20 | AD0 | O | ATA_ADR0 (on A16); → 22 Ω; 5 V |
| 21 | DD0 | IO | → 33 Ω; 5 V |
| 22 | DD1 | IO | → 33 Ω; 5 V |
| 23 | DD2 | IO | → 33 Ω; 5 V |
| 24 | IOCS16# | O | ↑ 1 kΩ, → 0 Ω (not used on module) |
| 25 | CD2# (N.C.) | – | NC |
| 26 | CD1# (N.C.) | – | NC |
| 27 | DD11 | I/O | → 33 Ω; 5 V |
| 28 | DD12 | I/O | → 33 Ω; 5 V |
| 29 | DD13 | I/O | → 33 Ω; 5 V |
| 30 | DD14 | I/O | → 33 Ω; 5 V |
| 31 | DD15 | I/O | → 33 Ω; 5 V |
| 32 | CS1# | O | ATA_CS1# (on LP_CS5#); → 22 Ω; 5 V |
| 33 | VS1# (N.C.) | – | NC |
| 34 | IOR# | O | ATA_IOR#; → 22 Ω; 5 V |
| 35 | IOWR# | O | ATA_IOWR#, → 22 Ω; 5 V |
| 36 | VCC5V | – | VCC5V |
| 37 | INTFL | I | ATA_INTRQ2 → 82 Ω; 5 V, ↓ 10 kΩ DGND |
| 38 | VCC5V | – | VCC5V |
| 39 | Select | O | CF Master/Slave jumper X79 (close = Master, open = Slave) |
| 40 | VS2# (N.C.) | – | NC |
| 41 | Reset# | O | /ATA_RES from Module (HW-Reset or SW-Reset (PSC1.4) → 22 Ω; 5 V |
| 42 | IOCHRDY | I | ATA_ IOCHRDY, → 82 Ω; 5 V |
| 43 | N.C. | – | NC |
| 44 | VCC5V | – | VCC5V |
| 45 | FLACT | I | Input for HDD activity → 22 Ω; 5 V, optional PSC3.0 |
| 46 | /CBLIDFL | O | ↓ 100 kΩ to GND, ↓ 47 nF to GND, → 0 Ω, optional PSC3.2 |
| 47 | DD8 | I/O | → 33 Ω; 5 V |
| 48 | DD9 | I/O | → 33 Ω; 5 V |
| 49 | DD10 | I/O | DGND |
| 50 | DGND | – | DGND |

# - Low active signal, ↑ - element to VCC (pull up), ↓ - element to ground (pull down), → element in series

Table 18: Pin Assignment Compact Flash Interface (X50)

Primary Master or Slave can be selected with jumper (X79).

## 4.2 Module-Interfaces on the Starterkit

All interfaces of the module are also routed to 2.54 mm headers on the Starterkit.

| Header | Interface |
|---|---|
| X2 | RS232-1 and RS232-2 |
| X6 | Ethernet |
| X11 | Ext. AD-Bus |
| X12 | PCI Ctrl pins |
| X14 | PLD-JTAG |
| X22 | Local Plus Bus CTRL, ATA-CTRL |
| X23 | PSC1, PSC2 |
| X24 | PSC3 |
| X25 | USB1 host |
| X26 | Reset, IRQ |
| X27 | Timer-Port |
| X28 | PSC6 |
| X29 | MPC52xx JTAG |
| X40 | GPIO (only in modules with graphics controller) |
| X43 | I²C1, I²C2 |
| X49 | Graphics controller CRT, USB Device (only modules with graphics controller) |
| X51 | JTAG/COP MPC52xx |
| X54 | Flat panel (only in modules with graphics controller) |
| X61 | Reserve (not equipped) |
| X71 | Reset |

Table 19: Pin Assignment I/Os

## 4.3 Internal Interfaces

### 4.3.1 Reset

A reset can be initiated using the reset switch S1. With this, the TQM5200 and the Starterkit are reset.

A red LED on the TQM5200 module shows the reset status.

### 4.3.2 Human Interface (16 LEDs)

On the STK52xx, 16 red LEDs are connected with drivers (74LVC244A). By setting jumper (X15) the driver can be activated. The first eight LEDs are assigned to the following processor ports:

- LED 0,1,2,3 – PSC3.0, PSC3.1, PSC3.2, PSC3.3
- LED 4,5,6,7 – Timer4, Timer5, Timer6, Timer7

The other eight LEDs are assigned to graphics controller ports:

- GPIO24, GPIO25, GPIO26, GPIO27, GPIO48, GPIO49, GPIO50, GPIO51

While using the Module without graphics controller, the last eight LEDs cannot be used.

It should also be noted that if the ports PSC3.0 to PSC3.3 are used for other purposes (e.g. for IDE Port or for using the second RS232 interface) with activated LED driver, the LEDs display the respective signal conditions of the corresponding ports.

### 4.3.3 Module Connector (D2.X1 – D2.X4)

120 pin and 40 pin Board-to-Board connectors with 0.8 mm pitch are used.

These connectors are available in different heights.

| Board-to-Board Distance | Base Board Connector | | |
|---|---|---|---|
| | No. of Pins | Supplier | Order No. |
| 5 mm | 40 | tyco | 177984-1 |
| 6 mm | 40 | tyco | 179029-1 |
| 7 mm | 40 | tyco | 179030-1 |
| 8 mm | 40 | tyco | 179031-1 |
| 5 mm | 120 | tyco | 177984-5 |
| 6 mm | 120 | tyco | 179029-5 |
| 7 mm | 120 | tyco | 179030-5 |
| 8 mm | 120 | tyco | 179031-5 |

Table 20: Base Board Connectors

#### 4.3.3.1 Pin Assignment Connector D2-X1

| Group | Function | MPC5200 BALL | Pin No. D2-X1 | | MPC5200 BALL | Function | Group |
|---|---|---|---|---|---|---|---|
| Power | GND | - | 2 | 1 | - | 3.3 V | Power |
| Ethernet | ETH_16 | L02 | 4 | 3 | J04 | ETH_17 | Ethernet |
| | ETH_14 | N04 | 6 | 5 | N03 | ETH_15 | |
| | ETH_12 | M02 | 8 | 7 | M01 | ETH_13 | |
| Power | GND | - | 10 | 9 | L04 | ETH_11 | |
| Ethernet | ETH_10 | J03 | 12 | 11 | L01 | ETH_9 | |
| | ETH_8 | M03 | 14 | 13 | - | 3.3 V | Power |
| | ETH_6 | N02 | 16 | 15 | N01 | ETH_7 | Ethernet |
| Power | GND | - | 18 | 17 | L03 | ETH_5 | |
| Ethernet | ETH_4 | J02 | 20 | 19 | J01 | ETH_3 | |
| | ETH_2 | K03 | 22 | 21 | K02 | ETH_1 | |
| | ETH_0 | K01 | 24 | 23 | R01 | IRQ3 | Interrupt |
| Power | GND | - | 26 | 25 | - | 3.3 V | Power |
| Interrupt | IRQ2 | P02 | 28 | 27 | P01 | IRQ1 | Interrupt |
| | IRQ0 | P03 | 30 | 29 | V06 | PCI_STOP# | PCI Control |
| PCI Control | PCI_TRDY# | W05 | 32 | 31 | R02 | PCI_RESET# | |
| Power | GND | - | 34 | 33 | Y07 | PCI_PERR# | |
| PCI Control | PCI_SERR# | W08 | 36 | 35 | Y06 | PCI_IRDY# | |
| | PCI_REQ# | U01 | 38 | 37 | - | 3.3 V | Power |
| | PCI_PAR | V07 | 40 | 39 | R04 | PCI_GNT# | PCI Control |
| Power | GND | - | 42 | 41 | W07 | PCI_DEVSEL# | |
| PCI | PCI_ID_SEL | U02 | 44 | 43 | Y02 | PCI_CBE_3# | |
| | PCI_FRAME# | V05 | 46 | 45 | W06 | PCI_CBE_2# | |
| | PCI_CLOCK | T01 | 48 | 47 | Y08 | PCI_CBE_1# | |
| Power | GND | - | 50 | 49 | - | 3.3 V | Power |
| PCI / ATA / LP AD-Bus | EXT_AD_30 | R03 | 52 | 51 | W10 | PCI_CBE_0# | PCI Control |
| | EXT_AD_28 | T03 | 54 | 53 | V01 | EXT_AD_31 | PCI / ATA / LP AD-Bus |
| | EXT_AD_26 | T02 | 56 | 55 | W01 | EXT_AD_29 | |
| Power | GND | - | 58 | 57 | Y01 | EXT_AD_27 | |
| PCI / ATA / LP AD-Bus | EXT_AD_24 | U03 | 60 | 59 | W02 | EXT_AD_25 | |
| | EXT_AD_22 | V03 | 62 | 61 | - | 3.3 V | Power |
| | EXT_AD_20 | V02 | 64 | 63 | W03 | EXT_AD_23 | PCI / ATA / LP AD-Bus |
| Power | GND | - | 66 | 65 | Y03 | EXT_AD_21 | |
| PCI / ATA / LP AD-Bus | EXT_AD_18 | V04 | 68 | 67 | Y04 | EXT_AD_19 | |
| | EXT_AD_16 | W04 | 70 | 69 | Y05 | EXT_AD_17 | |
| | EXT_AD_14 | W09 | 72 | 71 | U08 | EXT_AD_15 | |
| Power | GND | - | 74 | 73 | - | 3.3 V | Power |
| PCI / ATA / LP AD-Bus | EXT_AD_12 | Y09 | 76 | 75 | V08 | EXT_AD_13 | PCI / ATA / LP AD-Bus |
| | EXT_AD_10 | Y10 | 78 | 77 | V09 | EXT_AD_11 | |
| | EXT_AD_8 | W11 | 80 | 79 | V10 | EXT_AD_9 | |
| Power | GND | - | 82 | 81 | Y11 | EXT_AD_7 | |
| PCI / ATA / LP AD-Bus | EXT_AD_6 | U11 | 84 | 83 | W12 | EXT_AD_5 | |
| | EXT_AD_4 | V11 | 86 | 85 | - | 3.3 V | Power |
| | EXT_AD_2 | V12 | 88 | 87 | Y23 | EXT_AD_3 | PCI / ATA / LP AD-Bus |
| Power | GND | - | 90 | 89 | W13 | EXT_AD_1 | |
| PCI / ATA / LP AD-Bus | EXT_AD_0 | V13 | 92 | 91 | W16 | LP_RW | LP Control |
| LP Control | LP_TS# | Y13 | 94 | 93 | V14 | LP_ALE# | |
| ATA Control | LP_OE# | D08 | 96 | 95 | U14 | LP_ACK# | |
| Power | GND | - | 98 | 97 | - | 3.3 V | Power |
| ATA Control | ATA_IOR# | Y17 | 100 | 99 | Y16 | ATA_ISOLATION | ATA Control |
| | ATA_INTRQ | Y19 | 102 | 101 | W17 | ATA_IOW# | |
| | ATA_DACK# | Y18 | 104 | 103 | W18 | ATA_IOCHRDY | |
| Power | GND | - | 106 | 105 | V17 | ATA_DRQ | |
| CS# | LP_CS5# | V16 | 108 | 107 | non CPU | ATA_Reset# | |
| | LP_CS4# | Y15 | 110 | 109 | - | 3.3 V | Power |
| | LP_CS2# | V15 | 112 | 111 | W15 | LP_CS3# | CS# |
| Power | GND | - | 114 | 113 | Y14 | LP_CS1# | |
| CS# | LP_CS0# | W14 | 116 | 115 | - | *Reserve 19* | Reserve |
| Reserve | *Reserve 20* | - | 118 | 117 | Non CPU | Start_L_H | Boot Ctrl |
| Power | GND | - | 120 | 119 | - | 3.3 V | Power |

Table 21: Pin Assignment Connector D2-X1 (Base Module Connector 1)

#### 4.3.3.2 Pin Assignment Connector D2-X3

| Group | Function | MPC5200 BALL | Pin No. D2-X3 | | MPC5200 BALL | Function | Group |
|---|---|---|---|---|---|---|---|
| Power | GND | - | 2 | 1 | - | 3.3 V | Power |
| Reset | RESIN# | non CPU | 4 | 3 | B13 | HRESET# | Reset |
| | SRESET# | A14 | 6 | 5 | A13 | PO_RESET# | |
| CPU JTAG | CPU_JTAG_TDO | A02 | 8 | 7 | A04 | CPU_JTAG_TMS | CPU JTAG |
| Power | GND | - | 10 | 9 | A03 | CPU_JTAG_TDI | |
| CPU JTAG | TEST_SEL_1 | C03 | 12 | 11 | B03 | JCPU_JTAG_TRST# | |
| | CPU_JTAG_TCK | B04 | 14 | 13 | - | 3.3 V | Power |
| | TEST_SEL_0 | B01 | 16 | 15 | A01 | Test_Mode1 | CPU JTAG |
| Power | GND | - | 18 | 17 | B02 | Test_Mode0 | |
| USB1 | USB1_0 | H01 | 20 | 19 | H02 | USB1_1 | USB1 |
| | USB1_2 | H03 | 22 | 21 | G01 | USB1_3 | |
| | USB1_4 | G02 | 24 | 23 | G03 | USB1_5 | |
| Power | GND | - | 26 | 25 | - | 3.3 V | Power |
| USB1 | USB1_6 | G04 | 28 | 27 | F01 | USB1_7 | USB1 |
| | USB1_8 | F02 | 30 | 29 | F03 | USB1_9 | |
| Timer | TIMER_0 | Y20 | 32 | 31 | V18 | TIMER_1 | Timer |
| Power | GND | - | 34 | 33 | D02 | TIMER_3 | |
| Timer | TIMER_2 | D03 | 36 | 35 | E03 | TIMER_5 | |
| | TIMER_4 | D01 | 38 | 37 | - | 3.3 V | Power |
| | TIMER_6 | E02 | 40 | 39 | E01 | TIMER_7 | Timer |
| Power | GND | - | 42 | 41 | C04 | PSC3_9 | PSC 3 |
| PSC 3 | PSC3_8 | A05 | 44 | 43 | B05 | PSC3_7 | |
| | PSC3_6 | C05 | 46 | 45 | A06 | PSC3_5 | |
| | PSC3_4 | B06 | 48 | 47 | C06 | PSC3_3 | |
| Power | GND | - | 50 | 49 | - | 3.3 V | Power |
| PSC 3 | PSC3_2 | A07 | 52 | 51 | B07 | PSC3_1 | PSC 3 |
| PSC 2 | PSC2_4 | A08 | 54 | 53 | C07 | PSC3_0 | |
| | PSC2_2 | A09 | 56 | 55 | B08 | PSC2_3 | PSC 2 |
| Power | GND | - | 58 | 57 | B09 | PSC2_1 | |
| PSC 2 | PSC2_0 | C09 | 60 | 59 | B10 | PSC1_3 | PSC1 |
| PSC 1 | PSC1_4 / ATA-SW-Reset | A10 | 62 | 61 | - | 3.3 V | Power |
| | PSC1_2 | C10 | 64 | 63 | A11 | PSC1_1 | PSC1 |
| Power | GND | - | 66 | 65 | B11 | PSC1_0 | |
| PSC 6 | PSC6_2 | A12 | 68 | 67 | C13 | PSC6_3 | PSC 6 |
| | PSC6_0 | B12 | 70 | 69 | C11 | PSC6_1 | |
| RS232 | RS232 TxD_1 | non CPU | 72 | 71 | non CPU | RS232 RxD_1 | RS232 |
| Power | GND | - | 74 | 73 | - | 3.3 V | Power |
| RS232 | RS232 TxD_2 | non CPU | 76 | 75 | non CPU | RS232 RxD_2 | RS232 |
| I²C | SCL_2 | V20 | 78 | 77 | W20 | SDA_2 | I²C |
| | SCL_1 | V19 | 80 | 79 | W19 | SDA_1 | |
| Power | GND | - | 82 | 81 | non CPU | WP#/ACC | Flash Reset |
| GPIO | GPIO_WKUP_7 | C12 | 84 | 83 | non CPU | HRESETF# | |
| Battery | Vbatt 3V3 | non CPU | 86 | 85 | - | 3.3 V | Power |
| LP_Byte Select | SEL_B0# | non CPU | 88 | 87 | non CPU | SEL_B1 | LP_Byte Select |
| Power | GND | - | 90 | 89 | non CPU | SEL_B2 | |
| LP_Byte Select | SEL_B3# | non CPU | 92 | 91 | - | *Reserve 1* | Reserve |
| Reserve | *Reserve 2* | - | 94 | 93 | - | *Reserve 3* | |
| | *Reserve 4* | - | 96 | 95 | - | *Reserve 5* | |
| Power | GND | - | 98 | 97 | - | 3.3 V | Power |
| Reserve | *Reserve 6* | - | 100 | 99 | - | *Reserve 7* | Reserve |
| | *Reserve 8* | - | 102 | 101 | - | *Reserve 9* | |
| | *Reserve 10* | - | 104 | 103 | - | *Reserve 11* | |
| Power | GND | - | 106 | 105 | - | *Reserve 12* | |
| Reserve | *Reserve 14* | - | 108 | 107 | - | *Reserve 13* | |
| | *Reserve 16* | - | 110 | 109 | - | 3.3 V | Power |
| | *Reserve 18* | - | 112 | 111 | - | *Reserve 15* | Reserve |
| Power | GND | - | 114 | 113 | - | *Reserve 17* | |
| PLD-JTAG | JTAG_TDO | non CPU | 116 | 115 | non CPU | JTAG_TDI | PLD-JTAG |
| | JTAG_TCK | non CPU | 118 | 117 | non CPU | JTAG_TMS | |
| Power | GND | - | 120 | 119 | - | 3.3 V | Power |

Table 22: Pin Assignment Connector D2-X3 (Base Module Connector 2)

#### 4.3.3.3 Pin Assignment Connector D2-X2

| Group | Function | SM501 BALL | Pin No. D2-X2 | | SM501 BALL | Function | Group |
|---|---|---|---|---|---|---|---|
| Power | GND | - | 2 | 1 | - | 3.3 V | Power |
| CLK_OF | SM501_CLKOF | - | 4 | 3 | AA14 | SM501_USB- | USB |
| Power | GND | - | 6 | 5 | AA15 | SM501_USB+ | |
| GPIO | GPIO25 | M20 | 8 | 7 | M19 | GPIO24 | GPIO |
| | GPIO27 | N18 | 10 | 9 | M21 | GPIO26 | |
| | GPIO46 | V19 | 12 | 11 | N19 | GPIO28 | |
| Power | GND | - | 14 | 13 | - | 3.3 V | Power |
| GPIO | GPIO48 | V21 | 16 | 15 | V20 | GPIO47 | GPIO |
| | GPIO50 | W17 | 18 | 17 | W16 | GPIO49 | |
| LCD Interface | GPIO63 | Z21 | 20 | 19 | W18 | GPIO51 | |
| Power | GND | - | 22 | 21 | Z20 | GPIO62 | LCD Interface |
| LCD Interface | FP_CLK | AA10 | 24 | 23 | W12 | VDEN | |
| | FP_EN | V11 | 26 | 25 | - | 3.3 V | Power |
| | FP_DISP | Y12 | 28 | 27 | V123 | BIAS | LCD Interface |
| Power | GND | - | 30 | 29 | Y11 | FP_HSYNC | |
| CRT Interface | BLUE | AA12 | 32 | 31 | W11 | FP_VSYNC | |
| | GREEN | AA13 | 34 | 33 | W13 | HSYNC | CRT Interface |
| | RED | Y13 | 36 | 35 | W14 | VSYNC | |
| Power | GND | - | 38 | 37 | - | 3.3 V | Power |
| | GND | - | 40 | 39 | - | 3.3 V | |

Table 23: Pin Assignment Connector D2-X2 (Graphics Board-to-Board Connector 1)

#### 4.3.3.4 Pin Assignment Connector D2-X4

| Group | Function | SM501 BALL | Pin No. D2-X4 | | SM501 BALL | Function | Group |
|---|---|---|---|---|---|---|---|
| Power | GND | - | 2 | 1 | - | 3.3 V | Power |
| LCD Interface | FP_22 | Y10 | 4 | 3 | W10 | FP_23 | LCD Interface |
| Power | GND | - | 6 | 5 | V9 | FP_21 | |
| LCD Interface | FP20 | W9 | 8 | 7 | Y9 | FP_19 | |
| | FP18 | AA9 | 10 | 9 | Z19 | FP_17 | |
| | FP_16 | Y21 | 12 | 11 | W8 | FP_15 | |
| Power | GND | - | 14 | 13 | - | 3.3 V | Power |
| LCD Interface | FP_14 | Y8 | 16 | 15 | AA8 | FP_13 | LCD Interface |
| | FP_12 | V7 | 18 | 17 | W7 | FP_11 | |
| | FP_10 | Y7 | 20 | 19 | Y20 | FP_09 | |
| Power | GND | - | 22 | 21 | AA7 | FP_07 | |
| LCD Interface | FP_8 | Y19 | 24 | 23 | Y6 | FP_05 | |
| | FP_6 | W6 | 26 | 25 | - | 3.3 V | Power |
| | FP_4 | AA6 | 28 | 27 | V5 | FP_03 | LCD Interface |
| Power | GND | - | 30 | 29 | Y18 | FP_01 | |
| LCD Interface | FP_2 | W5 | 32 | 31 | Y16 | GPIO55 | |
| | FP_0 | Y17 | 34 | 33 | N20 | GPIO29 | |
| | GPIO30 | Z21 | 36 | 35 | P19 | GPIO31 | |
| Power | GND | - | 38 | 37 | - | 3.3 V | Power |
| | GND | - | 40 | 39 | - | 3.3 V | |

Table 24: Pin Assignment Connector D2-X4 (Graphics Board-to-Board Connector 2)

## 4.4 Testing, Debugging and Programming Interfaces

### 4.4.1 PLD-JTAG Interface (X14)

On the Minimodule a Lattice PLD is assembled, which is used for internal purposes only. There is no useful functionality for the user.

### 4.4.2 JTAG/BDM Interface (X29)

The JTAG/BDM interface is also called JTAG/COP adaptor.

The pin assignment is as follows:

| Pin Number | MPC52xx JTAG / BDM |
|---|---|
| 1 | JTAG_TDO |
| 2 | (Pull-up) /QACK |
| 3 | JTAG_TDI |
| 4 | /JTAG_TRST |
| 5 | (Pull-up) /QREQ (not used on board) |
| 6 | VCCS(10 mA), 3V3 |
| 7 | JTAG_TCK |
| 8 | N.C. (/PRESENT) |
| 9 | PLD_TMS |
| 10 | N.C. |
| 11 | /SRESET |
| 12 | DGND (N.C.) |
| 13 | /HRESET |
| 14 | N.C. (KEY, = coding pin, or to GND) |
| 15 | TEST_SEL_0 (/CKSTOP) / TEST_SEL_1 |
| 16 | DGND |

Table 25: JTAG/COP Lauterbach BDM Interface assignment (X29)

## 4.5 Additional Components on STK52xx

### 4.5.1 Buffer Battery

The TQM5200 module is optionally equipped with SRAM. On the STK52xx, an RTC is mounted. In order to buffer the data content of these components, a replaceable 3 V lithium battery is assembled on the STK52xx Starterkit as buffer battery.

| Manufacturer / Type | Description |
|---|---|
| Varta, Panasonic, Renata / CR2032 | 3 V / 235 mAh |

Table 26: Buffer Battery

The maximum power consumption of SRAM (15 µA) and RTC (1 µA) yields a power consumption of approximately 140 mAh per year. Through self-discharge of the battery, an additional 20 mAh per year are used. With these values a battery has a life expectancy of approx 1.5 years at 0 % operating time. The battery is used up after about 3 years at an average operating time of 50 %.

### 4.5.2 RTC

The ST Microelectronics M41T00 is used as RTC. The pin and register compatible Dallas DS 1340 is used optionally. The RTCs have the following features:

- I²C Interface
- Software clock calibration
- Counting of seconds, minutes, hours, days, months and years
- Automatic power fail detection and switching over to battery supply

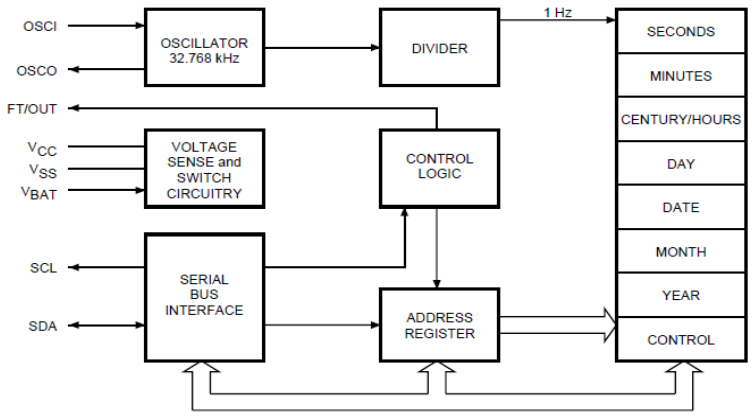


Illustration 9: RTC Block Diagram

The RTC is clocked by an oscillator with a frequency of 32.786 kHz. The RTC is connected to the MPC5200 via I²C-bus 2. The Pull-Up resistors to clock and data lines are not connected, as these are already present on the module at the I²C-EEPROM.

## 4.6 Jumper

The description of the jumper settings is given in the following table.

| Header | No. of Pins | Function | Default settings |
|---|---|---|---|
| X52 | 2 | PCI config / M66EN | Closed |
| X79 | 2 | MSTR select CF card | Open |
| X68 | 3 | MSTR select HDD | 2-3 closed |
| X13 | 2 | ETH IRQ | Open |
| X3 | 3 | ETH mode | 2-3 closed |
| X16 | 3 | ETH TXTSEW1 | 1-2 closed |
| X17 | 3 | ETH TXTSEW0 | 1-2 closed |
| X18 | 2 | ETH pause | Open |
| X5 | 2 | ETH PWRDWN | Open |
| X4 | 2 | ETH SLEEP | Open |
| X15 | 2 | LED_EN | Closed |
| X60 | 2 | USB1 disable | Open |
| X58 | 2 | USB host SOFTCON | Open |
| X62 | 2 | CAN1 TxD galvanic isolation | Open |
| X63 | 2 | CAN1 RxD galvanic isolation | Open |
| X9 | 2 | CAN1 transceiver speed mode | Open (High Speed) |
| X80 | 2 | CAN1 VCC galvanic isolation | Open |
| X85 | 2 | CAN1 GND galvanic isolation | Open |
| X65 | 2 | CAN2 TxD galvanic isolation | Open |
| X66 | 2 | CAN2 RxD galvanic isolation | Open |
| X10 | 2 | CAN2 transceiver speed mode | Open (High Speed) |
| X82 | 2 | CAN2 VCC galvanic isolation | Open |
| X86 | 2 | CAN2 GND galvanic isolation | Open |
| X64 | 3 | J1850 – ETH | 2-3 closed |
| X74 | 3 | J1850 – ETH | 2-3 closed |
| X76 | 3 | J1850 – ETH | 2-3 closed |
| X69 | 2 | J1850 RX galvanic isolation | Open |
| X78 | 2 | J1850 TX galvanic isolation | Open |
| X90 | 2 | J1850 12 V galvanic isolation | Open |
| X89 | 2 | J1850 GND galvanic isolation | Open |
| X72 | 3 | J1850 mode | Open |
| X37 | 3 | LCD backlight disable | Open |

Table 27: Jumper settings

## 4.7 Power Supply

The Starterkit can be supplied with the following voltages:

- 12 V ±10 % fuse protection with 4 A fuse (delivery status)
- 24 V ±25 % fuse protection with 2 A fuse

All other voltages are generated on the Starterkit using switching regulators.
Each voltage is protected with a self-resetting fuse.
If the STK52xx is powered with 12 V, these 12 V are directly supplied to the components on the STK52xx. Different LED's indicates the various internal voltages status.

- VCC3V3 = +3.3 V ±5 % for TQM5200 module and for STK52xx Starterkit
- VCC3V3P = +3.3 V ±5 % for PCI bus
- VCC5V = +5 V ±5 % for STK52xx Starterkit
- VCC5VP = +5 V ±5 % for PCI bus, IDE bus and backlight
- VCC12V = +12 V ±10 % for backlight and for J1850 interface

### 4.7.1 12 V / 24 V Connector (X19, X20)

Pin assignment of terminal block X20

| Pin | Signal | Description |
|---|---|---|
| 1 | VCC24V / VCC12V | VCC max. 2 A / max. 4 A |
| 2 | GND | Ground |

Table 28: Phoenix Terminal Block (X20)

Pin assignment of jack bush X19

| Pin | Signal | Description |
|---|---|---|
| Center | VCC24V / VCC12V | VCC max. 2 A / max. 2 A |
| Ring | GND | Ground |

Table 29: Jack Bush (X19)

To avoid overloading jack bush X19, it should only be used when no display backlight is supplied by the Starterkit.

### 4.7.2 Line Filter / Protective Circuit

Reverse battery protection at X20 and X19 up to –32 V.
The STK52xx is protected against damage through a voltage-controlled switch (PMOS).

| Manufacturer / Type | Description |
|---|---|
| Vishay, SUP65P04-15 VIS | P-Channel MOSFET, 60 V /IAR 60° / –55 °C to +175 °C |
| Wickmann / 181-4A | Fuse 4 A slow blow |
| General Semi / SMBJ30CA | Bidirectional suppressor diode; $U_{BR(min)}$ = 33.3 V |
| General Semi / SMBJ30A | Unidirectional suppressor diode; $U_{BR(min)}$ = 33.3 V |
| Vishay, F1750-012-112 | Noise suppression choke, IN = 10 A, L = 2.5 µH |

Table 30: Line Filter Components

# 5. Mechanical Specification

The overall dimensions of the STK52xx are 220 mm × 160 mm.

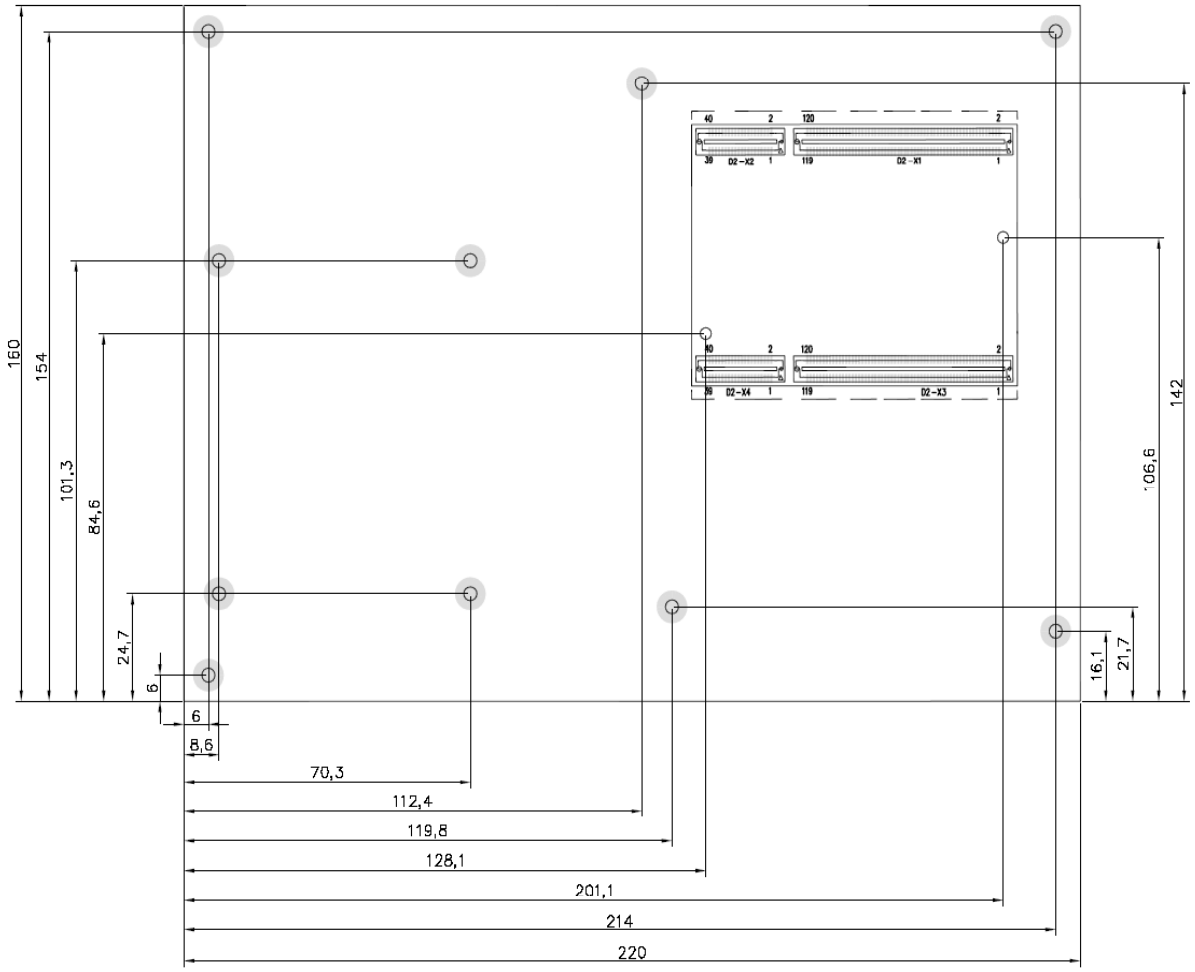


Illustration 10: Dimensional Drawing STK52xx Rev20x

## 5.1 Mounting Holes

There are two holes available for mounting the TQM5200 on the STK52xx.

Holes are provided on all four corners and in the center of the STK52xx.
These holes are meant for mounting the STK52xx in a cabinet.
Alternatively, these holes can also be used for mounting standoffs and a display holder.

Furthermore, four holes are available for mounting a 2.5” hard disk drive.

## 5.2 Assembly

### 5.2.1 Top Side

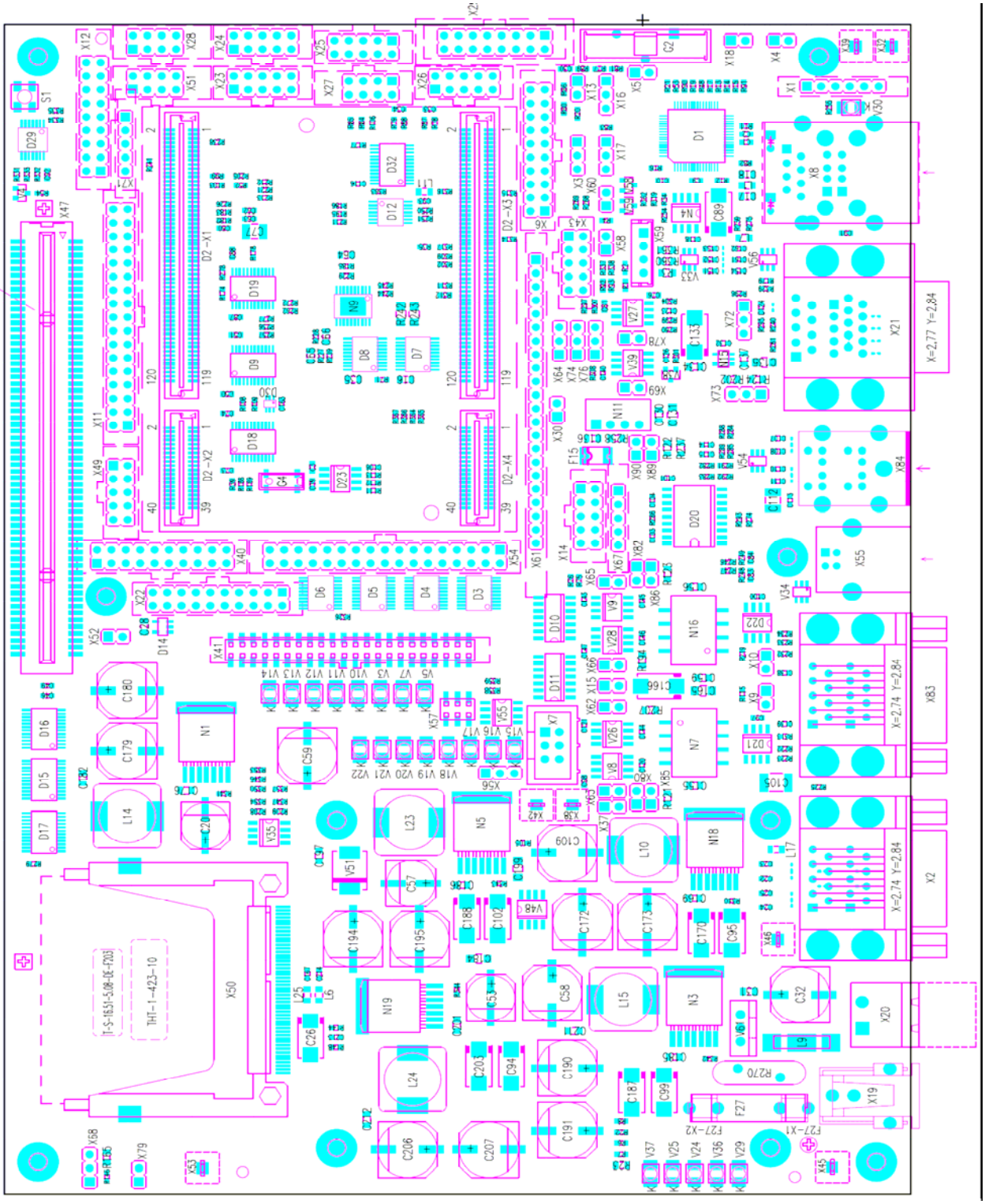

Illustration 11: Layout Diagram Top Side

### 5.2.2 Bottom Side

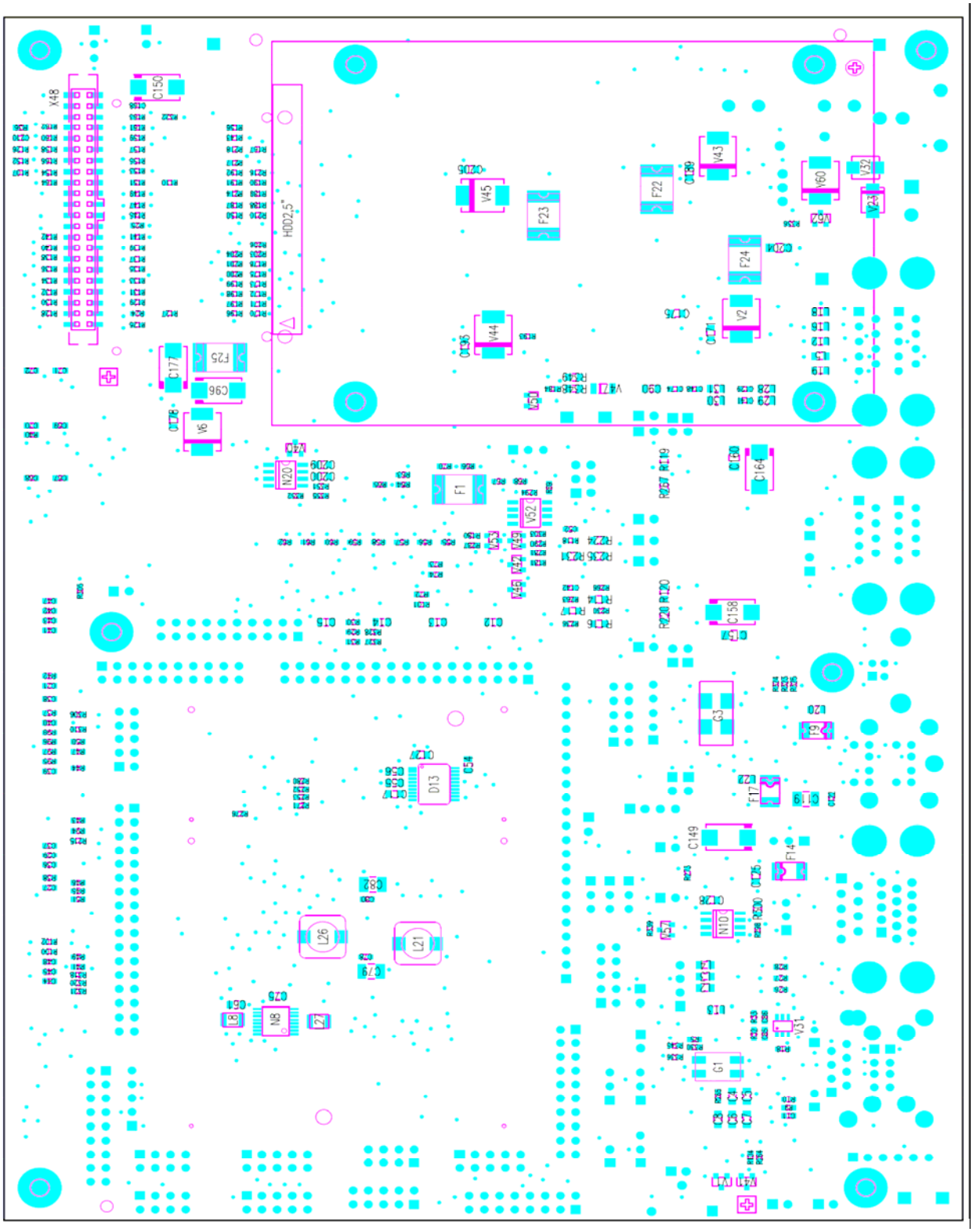


Illustration 12: Layout Diagram Bottom Side

# 6. Safety Requirements and Protective Regulations

## 6.1 Climate Conditions and Operational Conditions

- Protection class IP00
- Relative air humidity (operation / storing): 10 … 90 % (not condensing)
- Standard temperature range:
  - Chip temperature of the CPU: 0 °C to +60 °C
  - Package temperature of the remaining ICs: 0 °C to +60 °C
  - Storage temperature: –25 °C to +70 °C
- Extended temperature range:
  - Chip temperature of the CPU: –40 °C to +85 °C
  - Package temperature of the remaining ICs: –40 °C to +85 °C

## 6.2 Dependability and Durability / Service Life

The Components are designed for a typical service life of 5 years.

## 6.3 Environmental Protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

The energy consumption of this subassembly is minimised by suitable measures.

Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
(source of information: BGBl I 1994, 2705)

Regulation with respect to the utilization and proof of removal as at 1.9.96
(source of information: BGBl I 1996, 1382, (1997, 2860)

Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
(source of information: BGBl I 1998, 2379)

Regulation with respect to the European Waste Directory as at 1.12.01
(source of information: BGBl I 2001, 3379)

# 7. Appendix

## 7.1 Acronyms and Definitions

The following terminology and abbreviations are used:

| Acronym | Meaning |
|---|---|
| AC | Alternating Current |
| AD-Bus | Address/Data Bus |
| AGND | Analog Ground |
| ATA | Advanced Technology Attachment |
| BDM | Background Debug Mode |
| CAN | Controller Area Network |
| CF | Compact Flash |
| CODEC | Code/Decode |
| COP | Common On-chip Processor |
| CPU | Central Processing Unit |
| CRT | Cathode Ray Tube |
| DAC | Digital-to-Analog Converter |
| DC/DC | Direct Current/Direct Current |
| DGND | Digital Ground |
| DVI | Digital Visual Interface |
| ESD | ElectroStatic Discharge |
| ETH | Ethernet |
| FET | Field Effect Transistor |
| FP | Flat Panel |
| FR-4 | Flame Retardant 4 |
| I/O | Input/Output |
| IC | Integrated Circuit |
| IDE | Integrated Drive Electronics |
| I²C | Inter-Integrated Circuit |
| JTAG | Joint Test Action Group |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| LVDS | Low Voltage Differential Signal |
| Mbps | Megabit Per Second |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| N.C. | Not Connected |
| PCB | Printed Circuit Board |
| PCI | Peripheral Component Interconnect |
| PHY | Physical layer |
| PLD | Programmable Logic Device |
| PMOS | Positive Channel Metal Oxide Semiconductor |
| PS/2 | Personal System/2 |
| RTC | Real-Time Clock |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random Access Memory |
| TFT | Thin Film Transistor (display) |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |

Table 31: Acronyms

## 7.2 Literature

[1] TQM5200 User's Manual
TQM5200 UM 300, Rev. 300, 15.09.2010

[2] TQM5200S User's Manual
TQM5200S UM 300, Rev. 300, 04.09.2010

[3] MPC5200B User's Manual
MPC5200BUM Rev. 2 12/2008

[4] Linux Software Manual
LIN5200.SWM.106.pdf, Rev. 106, 10.02.2010