

**chcoze**

# DV-1000 Series

## User Manual



### Rugged Workstation

9/8th Generation Intel Core Series Processors, High Performance and Essential Rugged Embedded Computer

# Contents

Preface .....	5
Revision .....	5
Copyright Notice .....	5
Acknowledgement.....	5
Disclaimer .....	5
Declaration of Conformity .....	5
Product Warranty Statement .....	6
Technical Support and Assistance .....	7
Conventions Used in this Manual.....	8
Safety Precautions .....	8
Package Contents.....	9
Ordering Information .....	9
Chapter 1 .....	10
1.1 Overview .....	11
1.2 Highlights .....	11
1.3 Product pictures .....	13
1.4 Key Features.....	13
1.5 Hardware Specification .....	14
1.6 System I/O .....	18
1.7 Mechanical Dimension .....	20
Chapter 2.....	21
2.1 Location of Switches and Connectors .....	22
2.2 Switches and Connectors Definition .....	23
2.3 Switches Definition.....	25
2.4 Definition of Connectors .....	27
Chapter 3 .....	34
3.1 Removing the Top Cover .....	35
3.2 Installing the CPU .....	38
3.3 Installing SO-DIMM .....	40
3.4 Installing a Mini-PCIe/mSATA Card.....	41
3.5 Installing M.2 E Key Card.....	42
3.6 Installing M.2 M Key Card .....	43
3.7 Installing Antennas.....	44
3.8 Installing Top Cover .....	46
3.9 Installing SATA Hard Drive.....	46
3.10 Installing Bottom Cover .....	48
3.11 Removing the Front Cover Plate .....	48
3.12 Installing a SIM Card.....	49
3.13 Replacing the CMOS Battery .....	50

3.14 Fastening the Cover .....	52
3.15 Wall Mount Brackets .....	53
3.16 VESA Mount .....	54
<b>Chapter 4 .....</b>	<b>56</b>
<b>4.1 BIOS Introduction .....</b>	<b>57</b>
<b>4.2 Main Setup .....</b>	<b>58</b>
<b>4.2.1 System Date .....</b>	<b>58</b>
<b>4.2.2 System Time .....</b>	<b>58</b>
<b>4.3 Advanced Setup .....</b>	<b>59</b>
<b>4.3.1 CPU Configuration .....</b>	<b>59</b>
<b>4.3.2 Power &amp; Performance .....</b>	<b>60</b>
<b>4.3.3 SATA Configuration .....</b>	<b>60</b>
<b>4.3.4 PCH-FW Configuration .....</b>	<b>61</b>
<b>4.3.5 Trusted Computing Settings .....</b>	<b>62</b>
<b>4.3.6 ACPI Settings .....</b>	<b>63</b>
<b>4.3.7 F81866 Super IO Configuration .....</b>	<b>63</b>
<b>4.3.8 Hardware Monitor .....</b>	<b>65</b>
<b>4.3.9 S5 RTC Wake Settings .....</b>	<b>66</b>
<b>4.3.10 Serial Port Console Redirection .....</b>	<b>67</b>
<b>4.3.11 USB Configuration .....</b>	<b>67</b>
<b>4.3.12 Network Stack Configuration .....</b>	<b>68</b>
<b>4.3.13 CSM Configuration .....</b>	<b>69</b>
<b>4.3.14 NVMe Configuration .....</b>	<b>70</b>
<b>4.4 Chipset Setup .....</b>	<b>70</b>
<b>4.4.1 System Agent (SA) Configuration .....</b>	<b>71</b>
<b>4.4.2 PCH-IO Configuration .....</b>	<b>71</b>
<b>4.5 Security Setup .....</b>	<b>74</b>
<b>4.5.1 Administrator Password .....</b>	<b>74</b>
<b>4.5.2 User Password .....</b>	<b>74</b>
<b>4.6 Boot Setup .....</b>	<b>75</b>
<b>4.6.1 Setup Prompt Timeout .....</b>	<b>75</b>
<b>4.6.2 Bootup NumLock State .....</b>	<b>75</b>
<b>4.6.3 Quiet Boot .....</b>	<b>75</b>
<b>4.6.4 Fast Boot .....</b>	<b>75</b>
<b>4.6.5 Hard Drive BBS Priority .....</b>	<b>75</b>
<b>4.7 Save &amp; Exit .....</b>	<b>76</b>
<b>4.7.1 Save Changes and Exit .....</b>	<b>76</b>
<b>4.7.2 Discard Changes and Exit .....</b>	<b>76</b>
<b>4.7.3 Save Changes and Reset .....</b>	<b>76</b>
<b>4.7.4 Discard Changes and Reset .....</b>	<b>76</b>
<b>4.7.5 Save Changes .....</b>	<b>76</b>

4.7.6 Discard Changes .....	76
4.7.7 Restore Defaults.....	76
4.7.8 Save as User Defaults.....	76
4.7.9 Restore User Defaults .....	76
<b>Chapter 5.....</b>	<b>77</b>
5.1 Digital I/O (DIO) application.....	78
5.1.1 Digital I/O Programming Guide .....	78
5.2 DIO Hardware Specification .....	90
5.2.1 DIO Connector Definition.....	91
5.3 GPIO LED application .....	95
5.3.1 GPIO LED Programming Guide.....	95
5.4 GPIO LED Status Definition .....	100
<b>Chapter 6.....</b>	<b>101</b>
6.1 Optional Module Pin Definition & Settings .....	102
6.1.1 CMI-COM06 R10/UB1603 R10 Module .....	102
6.1.2 CFM-IGN04 R10 Module .....	104
6.2 Installing High Speed CMI Module .....	105
6.2.1 CMI-DP01-R10/UB1606-R10 Module .....	105
6.2.2 CMI-HD03-R10/UB1608-R10 Module .....	107
6.3 Installing Low Speed CMI Module .....	109
6.3.1 CMI-COM06-R10/UB1603-R10 .....	109
6.3.2 CMI-DIO06-R10/UB1618-R10 .....	111
6.4 Installing CFM Module.....	113
6.4.1 CFM-IGN04-R10.....	113
6.5 Installing MEC Module .....	114
6.5.1 MEC-USB-M102-15 /UB1614-R10.....	114
6.5.2 MEC-LAN-M102-15/UB1611-R10 .....	117
6.6 Installing Optional Accessories.....	120
6.6.1 DINRAIL-R10.....	120
6.6.2 FAN-EX104 .....	121

# Preface

# Revision

## Copyright Notice

© 2022 by Cincoze Co., Ltd. All rights are reserved. No parts of this manual may be copied, modified, or reproduced in any form or by any means for commercial use without the prior written permission of Cincoze Co., Ltd. All information and specification provided in this manual are for reference only and remain subject to change without prior notice.

## Acknowledgement

Cincoze is a registered trademark of Cincoze Co., Ltd. All registered trademarks and product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective owners.

## **Disclaimer**

This manual is intended to be used as a practical and informative guide only and is subject to change without notice. It does not represent a commitment on the part of Cincoze. This product might include unintentional technical or typographical errors. Changes are periodically made to the information herein to correct such errors, and these changes are incorporated into new editions of the publication.

# **Declaration of Conformity**



FCC

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when

the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.



## CE

The product(s) described in this manual complies with all application European Union (CE) directives if it has a CE marking. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques.

## Product Warranty Statement

### Warranty

Cincoze products are warranted by Cincoze Co., Ltd. to be free from defect in materials and workmanship for 2 years from the date of purchase by the original purchaser. During the warranty period, we shall, at our option, either repair or replace any product that proves to be defective under normal operation. Defects, malfunctions, or failures of the warranted product caused by damage resulting from natural disasters (such as by lightening, flood, earthquake, etc.), environmental and atmospheric disturbances, other external forces such as power line disturbances, plugging the board in under power, or incorrect cabling, and damage caused by misuse, abuse, and unauthorized alteration or repair, and the product in question is either software, or an expendable item (such as a fuse, battery, etc.), are not warranted.

### RMA

Before sending your product in, you will need to fill in Cincoze RMA Request Form and obtain an RMA number from us. Our staff is available at any time to provide you with the most friendly and immediate service.

#### ■ RMA Instruction

- Customers must fill in Cincoze Return Merchandise Authorization (RMA) Request Form and obtain an RMA number prior to returning a defective product to Cincoze for service.
- Customers must collect all the information about the problems encountered and note anything abnormal and describe the problems on the "Cincoze Service Form" for the RMA number apply process.
- Charges may be incurred for certain repairs. Cincoze will charge for repairs to products whose warranty period has expired. Cincoze will also charge for repairs to products if the damage resulted from acts of God, environmental or atmospheric disturbances, or other external forces through misuse, abuse, or unauthorized alteration or repair. If charges will be incurred for a repair,

Cincoze lists all charges, and will wait for customer's approval before performing the repair.

- Customers agree to ensure the product or assume the risk of loss or damage during transit, to prepay shipping charges, and to use the original shipping container or equivalent.
- Customers can be sent back the faulty products with or without accessories (manuals, cable, etc.) and any components from the system. If the components were suspected as part of the problems, please note clearly which components are included. Otherwise, Cincoze is not responsible for the devices/parts.
- Repaired items will be shipped along with a "Repair Report" detailing the findings and actions taken.

### **Limitation of Liability**

Cincoze' liability arising out of the manufacture, sale, or supplying of the product and its use, whether based on warranty, contract, negligence, product liability, or otherwise, shall not exceed the original selling price of the product. The remedies provided herein are the customer's sole and exclusive remedies. In no event shall Cincoze be liable for direct, indirect, special or consequential damages whether based on contract or any other legal theory.

### **Technical Support and Assistance**

1. Visit the Cincoze website at [www.cincoze.com](http://www.cincoze.com) where you can find the latest information about the product.
2. Contact your distributor or our technical support team or sales representative for technical support if you need additional assistance. Please have following information ready before you call:
  - Product name and serial number
  - Description of your peripheral attachments
  - Description of your software (operating system, version, application software, etc.)
  - A complete description of the problem
  - The exact wording of any error messages

## Conventions Used in this Manual



### WARNING

This indication alerts operators to an operation that, if not strictly observed, may result in severe injury.



### CAUTION

This indication alerts operators to an operation that, if not strictly observed, may result in safety hazards to personnel or damage to equipment.



### NOTE

This indication provides additional information to complete a task easily.

## Safety Precautions

Before installing and using this device, please note the following precautions.

1. Read these safety instructions carefully.
2. Keep this User's Manual for future reference.
3. Disconnect this equipment from any AC outlet before cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
8. Use a power cord that has been approved for using with the product and that it matches the voltage and current marked on the product's electrical range label. The voltage and current rating of the cord must be greater than the voltage and current rating marked on the product.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only

by qualified service personnel.

If one of the following situations arises, get the equipment checked by service personnel:

- The power cord or plug is damaged.
  - Liquid has penetrated into the equipment.
  - The equipment has been exposed to moisture.
  - The equipment does not work well, or you cannot get it work according to the user's manual.
  - The equipment has been dropped and damaged.
  - The equipment has obvious signs of breakage.
14. CAUTION: Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer.
15. Equipment intended only for use in a RESTRICTED ACCESS AREA.

## Package Contents

Before installation, please ensure all the items listed in the following table are included in the package.

Item	Description	Q'ty
1	DV-1000 Embedded System	1
2	CPU Thermal Pad	1
3	Utility DVD Driver	1
4	Screw Pack	1
5	Wall Mounting Kit	1
6	Power Terminal Block Connector	1
7	Remote Function Terminal Block Connector	1
8	External Fan Terminal Block Connector	1

Note: *Notify your sales representative if any of the above items are missing or damaged.*

## Ordering Information

Model No.	Product Description
DV-1000-R10	9/8th Generation Intel Core Series Processors, High Performance and Essential Rugged Embedded Computer



# **Chapter 1**

## **Product Introductions**

## 1.1 Overview

The DV-1000, with 9/8th Gen Intel® Core™ processor, is a fanless and rugged embedded computer optimized for edge computing applications. The high-performance DV-1000 processes data and makes real-time decisions at the edge, enabling enterprises to take immediate action on real-time data. The computer brings high-performance computing and industrial durability together in a compact footprint embedded computer, providing reliable long-time operation for mission-critical and space-limited applications in machine vision, manufacturing, railway infotainment, and smart city applications.

## 1.2 Highlights

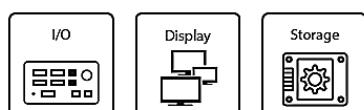


### Strong Computing Power

The DV-1000 features a 9/8th Generation Intel® Core™ i7/i5/i3 (Coffee Lake-R S series) processor and Intel® H310 chipset, supporting up to 128 GB of DDR4 2666 MHz memory. The DV-1000 provides plenty of power for heavy multitasking workloads and applications.

### Compact Size

The DV-1000 packs its impressive computing power in a compact size computer with a footprint only about half the size of one sheet of A4 paper. This small size makes the DV-1000 easy to install anywhere you can imagine, especially in space-constrained industrial environments like a small cabinet in a factory.



### Essential I/O and Connectivity

DV-1000 has the most frequently used I/O (LAN, USB, COM ports), analog and digital displays (DP and HDMI), and storage options (SATA HDD/SSD, mSATA, or NVMe) sufficient for most industrial applications.

## Expandable Extra I/O and Functionality

For adding extra I/O or functions Cincoze offers proprietary Combined Multiple I/O (CMI) modules, Control Function Module (CFM), and also Mini-PCIe Expansion Card Module (MEC). The CMI modules support high speed connectors such as HDMI and DisplayPort and low speed connectors such as COM and DIO, MEC modules support GbE LAN and USB expansion, and CFM modules have IGN function.



- 35W TDP Processor : -40°C to 70°C
- 65W TDP Processor : -40°C to 60°C (with external fan)

## Reliable Cooling and Wide Operating Temperature

Even in a small form factor, the DV-1000 has an excellent thermal design enabling wide operating temperature from -40°C to 70°C with only passive cooling. An external fan is available for an active cooling solution for higher temperature operations and to ensure continuous operation for space constraint cases or processing power requirements.

## Industry Certifications

The DV-1000 has been tested to meet a range of industry standards, including MIL-STD-810G to ensure reliable operation under harsh shock and vibration, and EMC compliance EN50155 (EN 50121-3-2 only) for rolling stock deployments.



EN50121-3-2



MIL-STD-810G

## 1.3 Product pictures



Front



Rear

## 1.4 Key Features

- Supports 9/8th Gen Intel® Core™ i7/i5/i3 or Pentium®/Celeron® processors (up to 65W)
- Compact size (224 x 162 x 64 mm)
- 1 x M.2 2280 key M socket, auto-detection for NVMe/SATA SSD
- 1 x M.2 2230 key E for Intel® CNVi/wireless module
- 2 x Full-size Mini PCIe sockets for module expansion
- Optional CMI/MEC modules for I/O expansion
- Wide operating temperature: -40°C to 70°C
- Military standard (MIL-STD-810G) shock & vibration proof
- Railway EMC standard EN50155 (EN 50121-3-2 only) certified

# 1.5 Hardware Specification

## System

Processor	<ul style="list-style-type: none"><li>• 9th Generation Intel® Coffee Lake-R S Series CPU:<ul style="list-style-type: none"><li>- Intel® Core™ i7-9700E 8 Cores Up to 4.4 GHz, TDP 65W</li><li>- Intel® Core™ i5-9500E 6 Cores Up to 4.2 GHz, TDP 65W</li><li>- Intel® Core™ i3-9100E 4 Cores Up to 3.7 GHz, TDP 65W</li><li>- Intel® Core™ i7-9700TE 8 Cores Up to 3.8 GHz, TDP 35W</li><li>- Intel® Core™ i5-9500TE 6 Cores Up to 3.6 GHz, TDP 35W</li><li>- Intel® Core™ i3-9100TE 4 Cores Up to 3.2 GHz, TDP 35W</li></ul></li><li>• 8th Generation Intel® Coffee Lake S Series CPU:<ul style="list-style-type: none"><li>- Intel® Core™ i7-8700 6 Cores Up to 4.6 GHz - 12M Cache, TDP 65W</li><li>- Intel® Core™ i5-8500 6 Cores Up to 4.1 GHz - 9M Cache, TDP 65W</li><li>- Intel® Core™ i3-8100 4 Cores 3.6 GHz - 6M Cache, TDP 65W</li><li>- Intel® Core™ i7-8700T 6 Cores Up to 4.0 GHz - 12M Cache, TDP 35W</li><li>- Intel® Core™ i5-8500T 6 Cores Up to 3.5 GHz - 9M Cache, TDP 35W</li><li>- Intel® Core™ i3-8100T 4 Cores 3.1 GHz - 6M Cache, TDP 35W</li><li>- Intel® Pentium® G5400 2 Cores 3.7 GHz - 4M Cache, TDP 58W</li><li>- Intel® Pentium® G5400T 2 Cores 3.1 GHz - 4M Cache, TDP 35W</li><li>- Intel® Celeron® G4900 2 Cores 3.1 GHz - 2M Cache, TDP 54W</li><li>- Intel® Celeron® G4900T 2 Cores 2.9 GHz - 2M Cache, TDP 35W</li></ul></li></ul>
Chipset	<ul style="list-style-type: none"><li>• Intel H310 Chipset</li></ul>
Memory	<ul style="list-style-type: none"><li>• 1x DDR4 2666 MHz 260-Pin SO-DIMM Socket, Supports Up to 32 GB ( Un-buffered and non-ECC)</li></ul>
BIOS	<ul style="list-style-type: none"><li>• AMI BIOS</li></ul>
<b>Graphics</b>	
Graphics Engine	<ul style="list-style-type: none"><li>• Integrated Intel® UHD Graphics 630: Core™ i7/i5/i3</li><li>• Integrated Intel® UHD Graphics 610: Pentium® /Celeron®</li></ul>
Maximum Display Output	<ul style="list-style-type: none"><li>• Supports Dual Independent Display</li></ul>
DP	<ul style="list-style-type: none"><li>• 1x DisplayPort Connector (4096 x 2304@60Hz)</li></ul>
VGA	<ul style="list-style-type: none"><li>• 1x VGA Connector (1920 x 1200 @60Hz)</li></ul>
<b>Audio</b>	
Audio Codec	<ul style="list-style-type: none"><li>• Realtek® ALC888, High Definition Audio</li></ul>
Line-out	<ul style="list-style-type: none"><li>• 1x Line-out, Phone Jack 3.5mm</li></ul>
Mic-in	<ul style="list-style-type: none"><li>• 1x Mic-in, Phone Jack 3.5mm</li></ul>

<b>I/O</b>	
LAN	<ul style="list-style-type: none"> <li>• 2x GbE LAN, RJ45               <ul style="list-style-type: none"> <li>- GbE1: Intel® I219</li> <li>- GbE2: Intel® I210</li> </ul> </li> </ul>
COM	<ul style="list-style-type: none"> <li>• 2x RS-232/422/485 with Auto Flow Control (Supports 5V/12V), DB9</li> </ul>
USB	<ul style="list-style-type: none"> <li>• 3x 5Gbps USB 3.2 Gen1, Type A</li> <li>• 3x 480Mbps USB 2.0, Type A</li> </ul>
<b>Storage</b>	
SSD/HDD	<ul style="list-style-type: none"> <li>• 1x 2.5" HDD/SSD Bay (SATA 3.0)</li> </ul>
mSATA	<ul style="list-style-type: none"> <li>• 2x mSATA Socket (SATA 3.0)</li> </ul>
M.2 SSD	<ul style="list-style-type: none"> <li>• 1x M.2 Key M 2280 Socket, Supports SATA SSD (SATA 3.0) and NVMe PCIe</li> </ul>
RAID	<ul style="list-style-type: none"> <li>• Do not Support RAID Function</li> </ul>
<b>Expansion</b>	
Mini PCI Express	<ul style="list-style-type: none"> <li>• 2x Full-size Mini-PCIe Socket</li> </ul>
SIM Socket	<ul style="list-style-type: none"> <li>• 1x SIM Socket</li> </ul>
M.2	<ul style="list-style-type: none"> <li>• 1x M.2 Key E 2230 Socket, Support Intel CNVi Module</li> </ul>
CMI (Combined Multiple I/O) Interface	<ul style="list-style-type: none"> <li>• 1x High Speed CMI Interface for optional CMI Module Expansion</li> <li>• 2x Low Speed CMI Interface for optional CMI Module Expansion</li> </ul>
CFM (Control Function Module) Interface	<ul style="list-style-type: none"> <li>• 1x CFM IGN Interface for optional CFM-IGN Module Expansion</li> </ul>
<b>Other Function</b>	
External FAN Connector	<ul style="list-style-type: none"> <li>• 1x External FAN Connector, 4-pin Terminal Block (Support Smart Fan by BIOS)</li> </ul>
Power Ignition Sensing	<ul style="list-style-type: none"> <li>• Support Power Ignition Sensing Function with Delay Time Management and Selectable 12V/24V (With Optional CFM Module)</li> </ul>
Clear CMOS Switch	<ul style="list-style-type: none"> <li>• 1x Clear CMOS Switch</li> </ul>
Reset Button	<ul style="list-style-type: none"> <li>• 1x Reset Button</li> </ul>
Instant Reboot	<ul style="list-style-type: none"> <li>• Support 0.2sec Instant Reboot Technology</li> </ul>
Watchdog Timer	<ul style="list-style-type: none"> <li>• Software Programmable Supports 256 Levels System Reset</li> </ul>

<b>Power</b>	
Power Button	<ul style="list-style-type: none"> <li>• 1x ATX Power On/Off Button</li> </ul>
Power Mode Switch	<ul style="list-style-type: none"> <li>• 1x AT/ATX Mode Switch</li> </ul>
Power Input	<ul style="list-style-type: none"> <li>• 9-48VDC, 3-pin Terminal Block</li> </ul>
Remote Power On/Off	<ul style="list-style-type: none"> <li>• 1x Remote Power On/Off, 2-pin Terminal Block</li> </ul>
Remote Power LED	<ul style="list-style-type: none"> <li>• 1x Remote Power LED, 2-pin Terminal Block</li> </ul>
<b>Physical</b>	
Dimension (W x D x H)	<ul style="list-style-type: none"> <li>• 224.1 x 162 x 64.2 mm</li> </ul>
Weight Information	<ul style="list-style-type: none"> <li>• 2.22 KG</li> </ul>
Mechanical Construction	<ul style="list-style-type: none"> <li>• Extruded Aluminum with Heavy Duty Metal</li> </ul>
Mounting	<ul style="list-style-type: none"> <li>• Wall/ DIN-RAIL/ VESA Mount</li> </ul>
Physical Design	<ul style="list-style-type: none"> <li>• Fanless Design</li> <li>• Cableless Design</li> <li>• Jumper-less Design</li> <li>• Unibody Design</li> </ul>
<b>Reliability &amp; Protection</b>	
Reverse Power Input Protection	<ul style="list-style-type: none"> <li>• Yes</li> </ul>
Over Voltage Protection	<ul style="list-style-type: none"> <li>• Protection Range: 51-58V</li> <li>• Protection Type: shut down operating voltage, re-power on at the present level to recover</li> </ul>
Over Current Protection	<ul style="list-style-type: none"> <li>• 15A</li> </ul>
Surge Protection	<ul style="list-style-type: none"> <li>• 2 kV</li> </ul>
CMOS Battery Backup	<ul style="list-style-type: none"> <li>• SuperCap Integrated for CMOS Battery Maintenance-free Operation</li> </ul>
MTBF	<ul style="list-style-type: none"> <li>• MTBF: 458,722 hours</li> <li>- Database: Telcordia SR-332 Issue3, Method 1, Case 3</li> </ul>
<b>Operating System</b>	
Windows	<ul style="list-style-type: none"> <li>• Windows® 10</li> </ul>
Linux	<ul style="list-style-type: none"> <li>• Supports by project</li> </ul>

## Environment

Operating Temperature	<ul style="list-style-type: none"><li>• 35W TDP Processor: -40°C to 70°C</li><li>• 65W TDP Processor: -40°C to 60°C (With External Fan Kit)<ul style="list-style-type: none"><li>- With extended temperature peripherals; Ambient with air flow</li><li>- According to IEC60068-2-1, IEC60068-2-2, IEC60068-2-14</li></ul></li></ul>
Storage Temperature	<ul style="list-style-type: none"><li>• -40°C to 85°C</li></ul>
Relative Humidity	<ul style="list-style-type: none"><li>• 95%RH @ 70°C (non-Condensing)</li></ul>
Shock	<ul style="list-style-type: none"><li>• MIL-STD-810G</li></ul>
Vibration	<ul style="list-style-type: none"><li>• MIL-STD-810G</li></ul>
EMC	<ul style="list-style-type: none"><li>• CE, FCC, ICES-003 Class A, EN50121-3-2 (Railway), E-mark</li></ul>
Safety	<ul style="list-style-type: none"><li>• IEC/EN 62368-1</li></ul>

\* *Product Specifications and features are for reference only and are subject to change without prior notice. For more information, please refer to the latest product datasheet from Cincoze's website.*

# 1.6 System I/O

## 1.6.1 Front

### ATX Power On/Off

Used to power-on or power-off the system

### Power LED

Indicates the power status of the system

### HDD LED

Indicates the status of the hard drive

### Temperature LED

Indicates the temperature of the system

### GPIO LED

Indicates the status of the GPIO

### USB 2.0

Used to connect USB 2.0/1.1 device

### USB 3.2 GEN1

Used to connect USB 3.2 GEN1/3.0/2.0/1.1 device

### Universal I/O Bracket

Used to customized I/O output with optional modules

### CMOS Battery

Used to clear CMOS to reset BIOS

### Clear CMOS Switch

Used to clear CMOS to reset BIOS

### IGN Setting Switch

Used to set up IGN function

### SIM

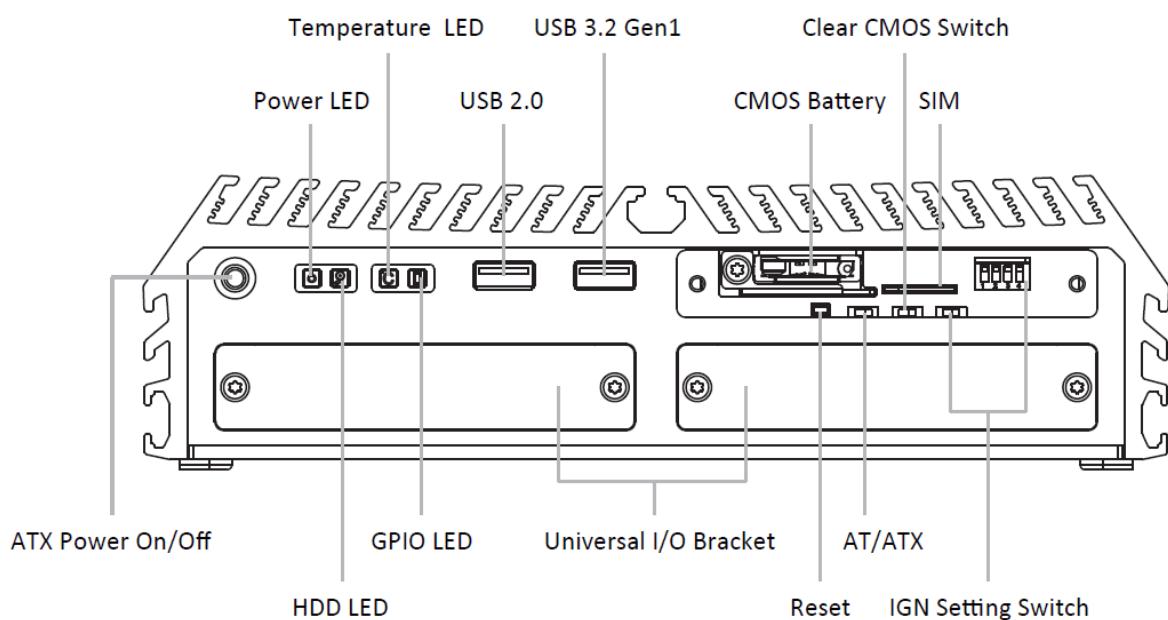
Used to insert a SIM card

### Reset

Used to reset the system

### AT/ATX

Used to select AT or ATX power mode



## 1.6.2 Rear

### DC Input

Used to plug a DC power input with terminal block

### Antenna

Used to connect an antenna for optional wireless module

### Chassis GND

Used to conduct static electricity to the ground

### External Fan Power

Used to plug an external fan with terminal block

### VGA

Used to connect a monitor with VGA interface

### DP

Used to connect a monitor with DisplayPort interface

### Remote Power On/Off

A terminal block used to connect to remote power on/off switch

### Remote Power LED

A terminal block used to connect to remote power on/off LED

### Line-Out

Used to connect a speaker

### Mic-In

Used to connect a microphone

### USB 2.0

Used to connect USB 2.0/1.1 device

### USB 3.2 GEN1

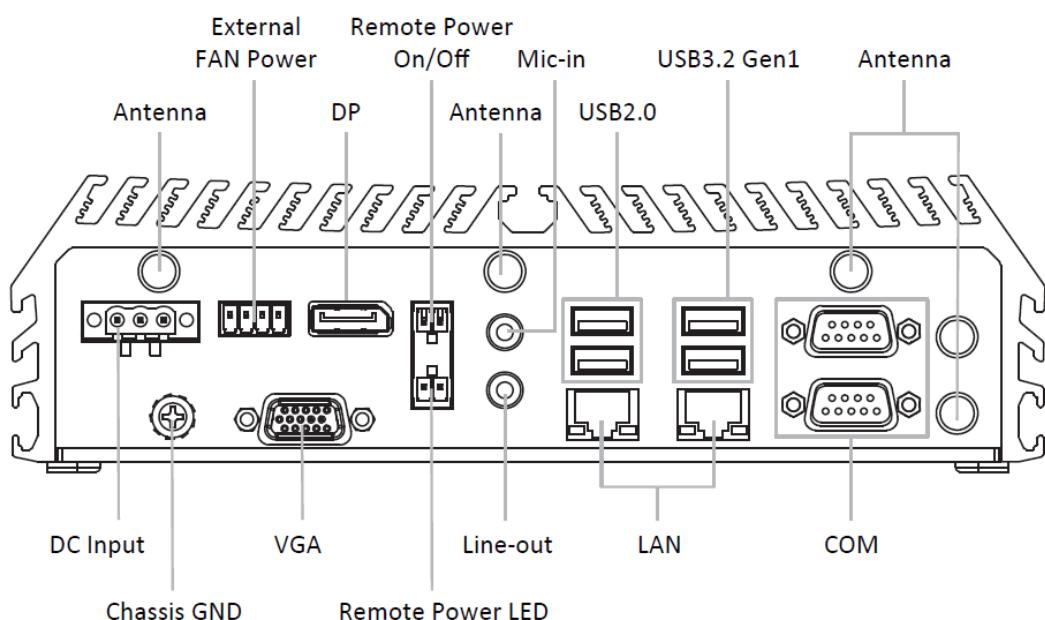
Used to connect USB 3.2 GEN1/3.0/2.0/1.1 device

### LAN

Used to connect to local area network

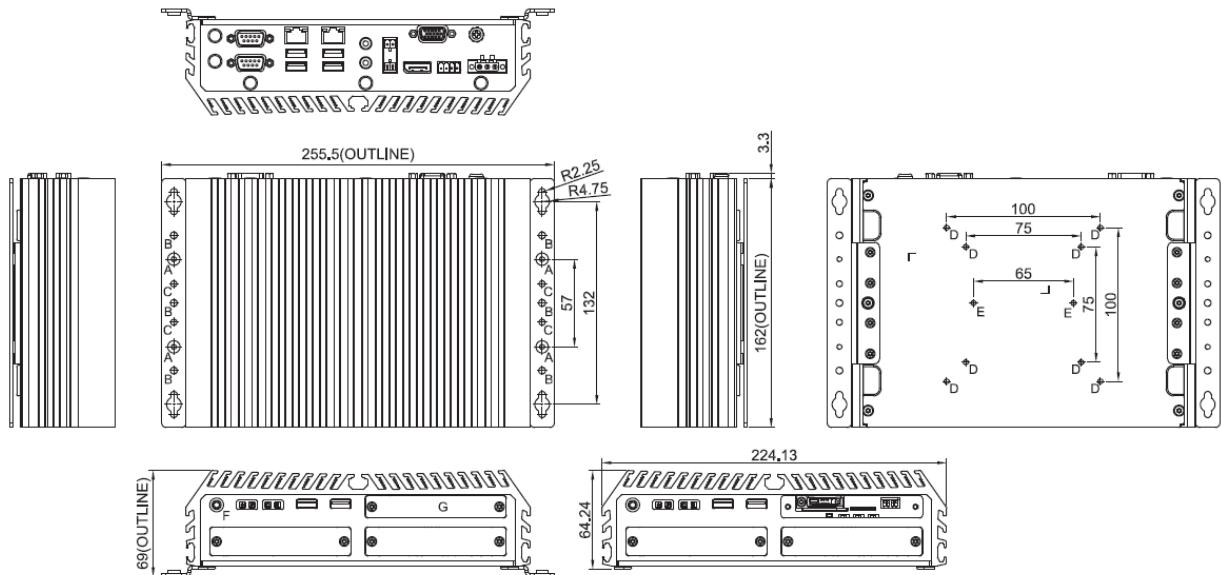
### COM

Used to connect to RS-232/422/485 serial devices



## 1.7 Mechanical Dimension

Unit: mm

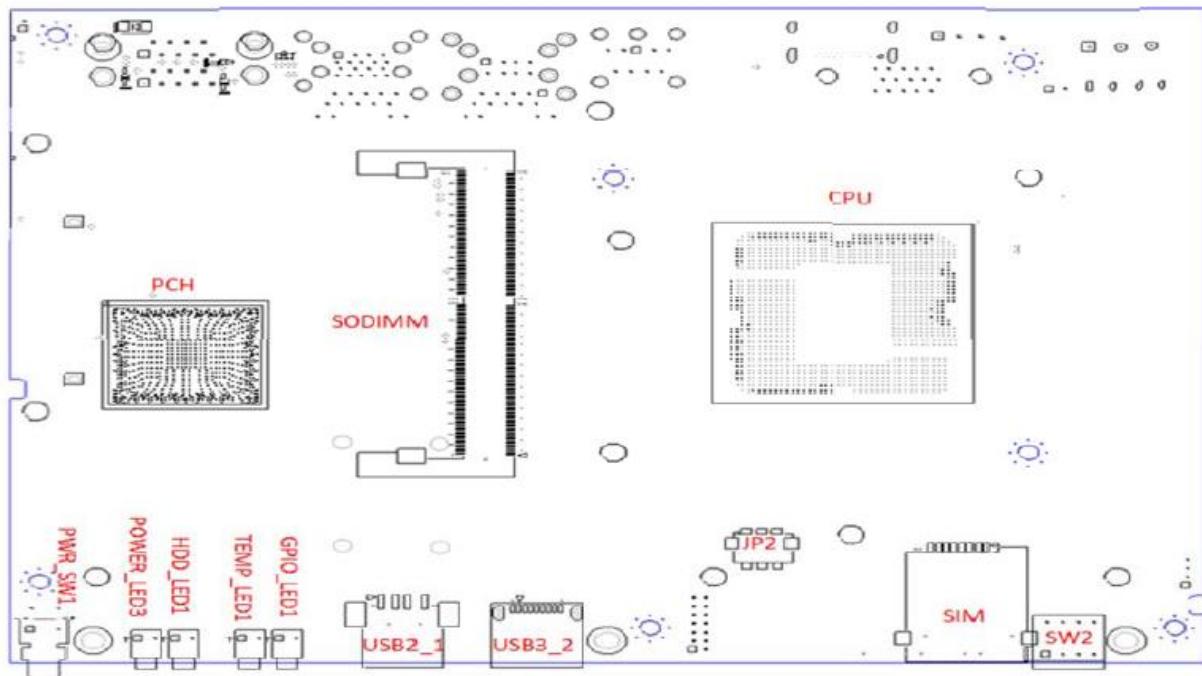


# **Chapter 2**

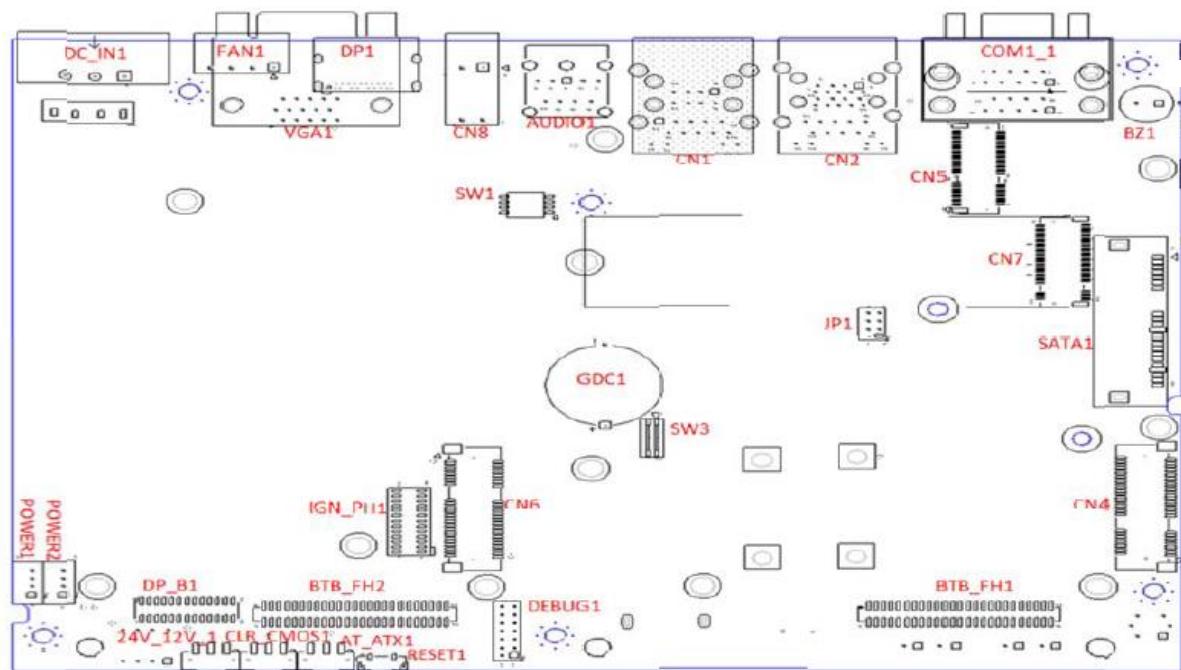
## **Switches & Connectors**

## 2.1 Location of Switches and Connectors

### 2.1.1 Top View



### 2.1.2 Bottom View



## 2.2 Switches and Connectors Definition

### 2.2.1 List of Switch

top view

Location	Definition
PWR_SW1	ATX Power Button Switch
SW2	IGN Module Timing Setting Switch (only functional with IGN module)

bottom view

Location	Definition
AT_ATX1	AT / ATX Power Mode Switch
SW1	COM1~2 Power Select Switch
SW3	Super CAP Switch
24V_12V_1	IGN Module Voltage Mode Setting Switch
Reset1	Reset Button
CLR_CMOS1	Clear BIOS Switch

## 2.2.2 List of Connector

### top view

Location	Definition
SODIMM	DDR4 SO-DIMM Slot
JP2	VBAT Connect
GPIO_LED1	GPIO LED
TEMP_LED1	Temperature LED (blue/red)
HDD_LED1	Hard disk LED (yellow blink)
POWER_LED3	Power LED (Green)
PCH	South bridge
CPU	CPU socket
USB2_1	USB2.0 connector
USB3_2	USB3.2 GEN1 connector
SIM	SIM card connector

### bottom view

Location	Definition
DC_IN1	DC power connector (+9-48V)
FAN1	Smart FAN connector
DP1	Display port connector
VGA1	VGA connector
CN8	Remote power on/off switch and power LED remote connector
AUDIO1	Audio head phone mic connector
CN1	LAN and USB2.0 X2 connector
CN2	LAN and USB3.2 GEN1 X2 connector
COM_1_1	DB9 connectors X2, support RS232/RS422/RS485
BZ1	BUZZER
CN5	M.2 Key E connector (support PCIE/CNVI interface)
CN7	M.2 KEY M connector
JP1	SPI ROM programming connector (Optional)
GDC1	Super cap
SATA1	SATA connector
POWER1/POWER2	Power connector
IGN_PH1	IGN connector
CN4	mini PCIE card connector (support mPCIE, mSATA interface)
CN6	mini PCIE card connector (support mPCIE, mSATA, USB3 interface)
DP_B1	DDI Signal connector support DP/HDMI (2K) interface
BTB_FH1/BTB_FH2	DIO or COM Port Board to Board Connector

## 2.3 Switches Definition

**PWR\_SW1: ATX Power on/off Button**

Switch	Definition
Push	Power on System



**AT\_ATX1: AT / ATX Power Mode Switch**

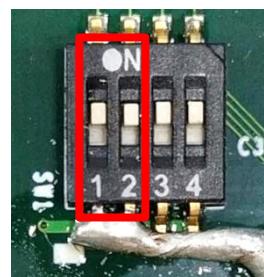
Switch	Definition
1-2 (Left)	AT Power Mode
2-3 (Right)	ATX Power Mode (Default)



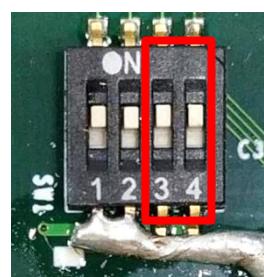
**SW1: COM1/COM2 Power Select**

COM1 / 2 Voltage Function Setting via DIP Switch

Location	Function	DIP1	DIP2
SW1	COM1	0V(RI)	ON (Default)
		5V	ON
		12V	OFF

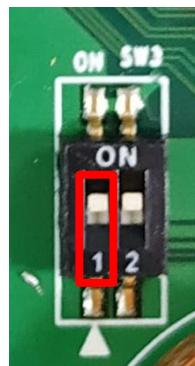


Location	Function	DIP3	DIP4
SW1	COM2	0V(RI)	ON (Default)
		5V	ON
		12V	OFF



**SW3: Super CAP Switch**

DIP	Function	ON	OFF
1	Super CAP	Enable (Default)	Disable
2	N/A	N/A	N/A



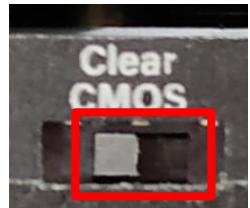
### **Reset1: System Reset Button**

<b>Button</b>	<b>Definition</b>	<b>Button</b>	<b>Definition</b>
Push	Reset System	Push	Reset System



### **CLR\_CMOS1: Clear CMOS Switch**

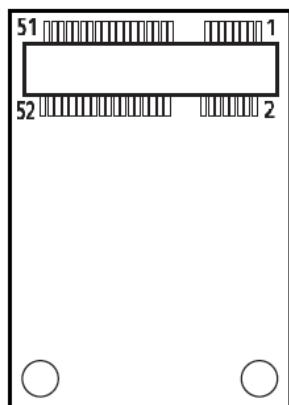
<b>Pin</b>	<b>Definition</b>
1-2 (Left)	Normal Status (Default)
2-3 (Right)	Clear CMOS



## 2.4 Definition of Connectors

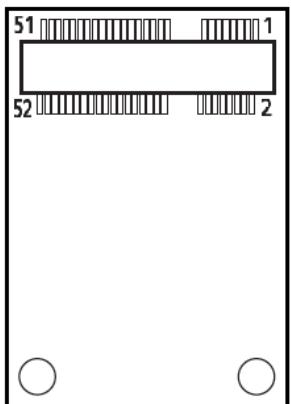
CN4: mini PCIE card connector (support mPCIE, mSATA interface)

Pin	Definition	Pin	Definition	Pin	Definition
1	WAKE#	19	NA	37	GND
2	3.3V	20	3.3V	38	USB_D+
3	NA	21	GND	39	3.3V
4	GND	22	PERST#	40	GND
5	NA	23	PERN/SATARP	41	3.3V
6	1.5V	24	+3.3VAUX	42	NA
7	CLKREQ#	25	PERP/SATARN	43	GND
8	NA	26	GND	44	NA
9	GND	27	GND	45	NA
10	NA	28	+1.5V	46	NA
11	REFCLK-	29	GND	47	NA
12	NA	30	SMB_CLK	48	+1.5V
13	REFCLK+	31	PETN/SATATN	49	NA
14	NA	32	SMB_DATA	50	GND
15	GND	33	PETP/SATATP	51	NA
16	NA	34	GND	52	+3.3V
17	NA	35	GND		
18	GND	36	USB_D-		



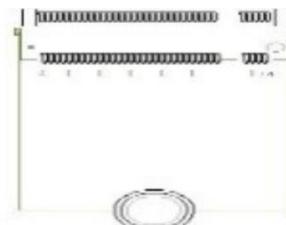
**CN6 : mini PCIE card connector (support mPCIE, mSATA, USB3 interface)**

Pin	Definition	Pin	Definition	Pin	Definition
1	WAKE#	19	SIM_DATA2	37	RESERVED
2	3.3V	20	3.3V	38	USB_D+
3	NA	21	GND	39	RESERVED
4	GND	22	PERST#	40	GND
5	NA	23	PERN/SATARP/ USB3RN	41	3.3V
6	1.5V	24	3.3V	42	NA
7	UIM_RST2	25	PERP/SATARN/ USB3RP	43	GND
8	SIM_PWR1	26	GND	44	NA
9	GND	27	GND	45	NA
10	SIM_DATA1	28	+1.5V	46	NA
11	REFCLK-	29	GND	47	NA
12	SIM_CLK	30	SMB_CLK	48	+1.5V
13	REFCLK+/SIM_PWR2	31	PETN/SATATN/ USB3TN	49	NA
14	SIM_Reset1	32	SMB_DATA	50	GND
15	GND	33	PETP/SATAP/ USB3TP	51	NA
16	SIM_VPP1	34	GND	52	+3.3V
17	SIM_CLK2	35	GND		
18	GND	36	USB_D-		



## CN5 : M.2 Key E connector (support PCIE/CNVI interface)

Pin	Definition	Pin	Definition	Pin	Definition
1	GND	27	KEY	53	N/A
2	+3.3V	28	KEY	54	W_DISABLE2# (Pull-up)
3	USB_D+	29	KEY	55	PEWAKE0#
4	+3.3V	30	KEY	56	W_DISABLE1# (Pull-up)
5	USB_D-	31	KEY	57	GND
6	N/A	32	UARTX/RGI_DT	58	I2C_DATA
7	GND	33	GND	59	WTD1N/PETP1
8	PCM_CLK	34	UART_CTS/RGI_RSP	60	I2C_CLK
9	N/A	35	PETP0	61	WTD1P/PETN1
10	PCM_SYNC/LPC_RST_N	36	UART_RTS/BRI_DT	62	N/A
11	N/A	37	PETN0	63	GND
12	PMC_IN	38	N/A	64	N/A
13	GND	39	GND	65	WTD0N/PETP1
14	USB3_TX4-	40	N/A	66	PERST1#
15	N/A	41	PERP0	67	WTD0P/PERN1
16	USB3_TX4+	42	N/A	68	CLKREQ1#
17	N/A	43	PERN0	69	GND
18	GND	44	N/A	70	PEWAKE1#
19	GND	45	GND	71	WTCLKN/REFCLKP1
20	UART_WAKE#	46	N/A	72	+3.3V
21	N/A	47	REFCLKP0	73	WTCLKP/REFCLKN1
22	UART_RX/BRI_RSP	48	N/A	74	+3.3V
23	N/A	49	REFCLKN0	75	GND
24	KEY	50	SUSCLK		
25	KEY	51	GND		
26	KEY	52	PERST0#		



## CN7 : M.2 Key M 2280 Socket (Support NVMe PCIe / SATA interface)

(pin 59 to pin 66 are connector keys)

Pin	Definition	Pin	Definition	Pin	Definition
1	CFG3	27	GND	53	REFCLKN
2	+3.3V	28	NC	54	PEWAKE#
3	GND	29	PERN1	55	REFCLKP
4	+3.3V	30	NC	56	NC
5	PERN3	31	PERP1	57	GND
6	NC	32	NC	58	NC
7	PERP3	33	GND	59	key
8	NC	34	NC	60	key
9	GND	35	PETN1	61	key
10	LED	36	NC	62	key
11	PETN3	37	PETP1	63	key
12	+3.3V	38	DEVSLP	64	key
13	PETP3	39	GND	65	key
14	+3.3V	40	SMB_CLK	66	key
15	GND	41	PERN0/SATARP0	67	NC
16	+3.3V	42	SMD_DATA	68	SUSCLK
17	PERN2	43	PERP0/SATARN0	69	PEDET
18	+3.3V	44	ALERT#	70	+3.3V
19	PERP2	45	GND	71	GND
20	NC	46	NC	72	+3.3V
21	CFG0	47	PETN0/SATATN0	73	GND
22	NC	48	NC	74	+3.3V
23	PETN2	49	PETP0/SATATP0	75	CFG2
24	NC	50	RESET#	76	NC
25	PETP2	51	GND		
26	NC	52	NC		



### **POWER\_LED3: Power LED Status**

Location	Status	LED Color
Power_LED3	Power ON	Green
	Standby	Blinking Green



Power LED

### **HDD\_LED1: Hard disk LED Status**

Location	Status	LED Color
HDD_LED1	HDD Read/Write	Blinking Yellow



HDD LED

### **TEMP\_LED1: Temperature LED Status**

Location	Status	LED Color
TEMP_LED1	System Temp $\leq$ 65°C	Colorless
	65°C < System Temp $\leq$ 70°C	Blue
	70°C < System Temp $\leq$ 75°C	Red
	75°C < System Temp	Blinking Red



NOTE

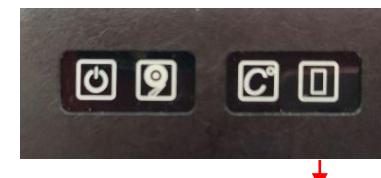
The TEMP LED is only available when IGN module is installed.



TEMP LED

### **GPIO\_LED1: Temperature LED Status**

Location	Status	LED Color
GPIO_LED1	GPIO activity	Green
	No activity	Off

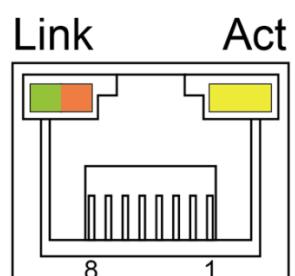


GPIO LED

### **CN1 / CN2: LAN1 / 2 LED Status Definition**

Act LED Status	Definition
Blinking Yellow	Data Activity
Off	No Activity

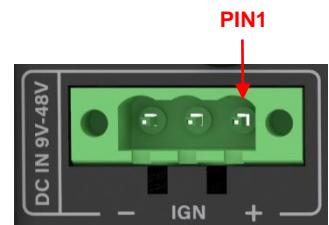
Link LED Status	Definition
Steady Green	1Gbps Network Link
Steady Orange	100Mbps Network Link
Off	10Mbps Network Link



## DC\_IN1: DC Power Input Connector (+9-48V)

Connector Type: Terminal Block 1x3 3-pin, 5.0mm pitch

Pin	Definition
1	+9-48VIN
2	Ignition (IGN)
3	GND



CAUTION

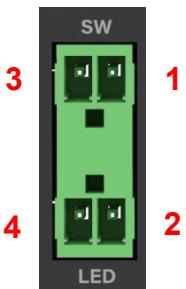
Please disconnect the power source before mounting the DC power cables or connecting the DC power connector to system.

## CN8: Remote power on/off switch and power LED remote connector

capable of connecting an external LED indicator up to 10mA.

Connector Type: Terminal Block 2X2 4-pin, 3.5mm pitch

Pin	Definition
1	PWR_SW
2	LED
3	GND
4	GND



WARNING

Do not apply power to this connector!  
This port is used to connect a SWITCH!

## FAN1: Smart Fan Connector

Connector Type: Terminal Block 1X4 4-pin, 3.5mm pitch

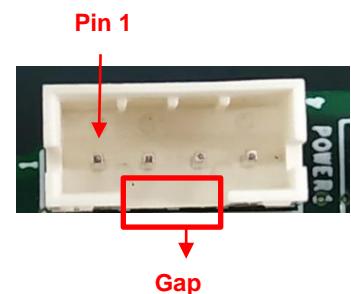
Pin	Definition
1	GND
2	+12V
3	SENSE
4	Control



## POWER1 / 2: Power Connector

Connector Type: 1x4 4-pin Wafer, 2.0mm pitch

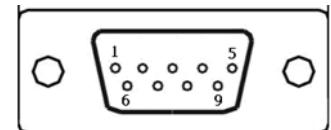
Pin	Definition
1	+5V
2	GND
3	GND
4	+12V



## COM1 / COM2: RS232 / RS422 / RS485 Connector

Connector Type: 9-pin D-Sub

Pin	RS232 Definition	RS422 / 485 Full Duplex Definition	RS485 Half Duplex Definition
1	DCD	TX-	DATA -
2	RXD	TX+	DATA +
3	TXD	RX+	
4	DTR	RX-	
5		GND	
6	DSR		
7	RTS		
8	CTS		
9	RI		



# **Chapter 3**

## **System Setup**

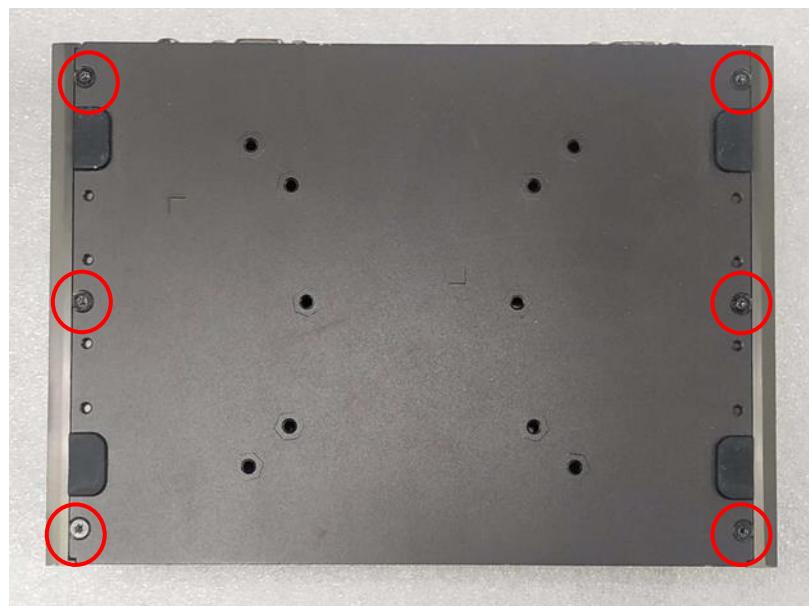
### 3.1 Removing the Top Cover



#### WARNING

In order to prevent electric shock or system damage, before removing the chassis cover, must turn off power and disconnect the unit from power source.

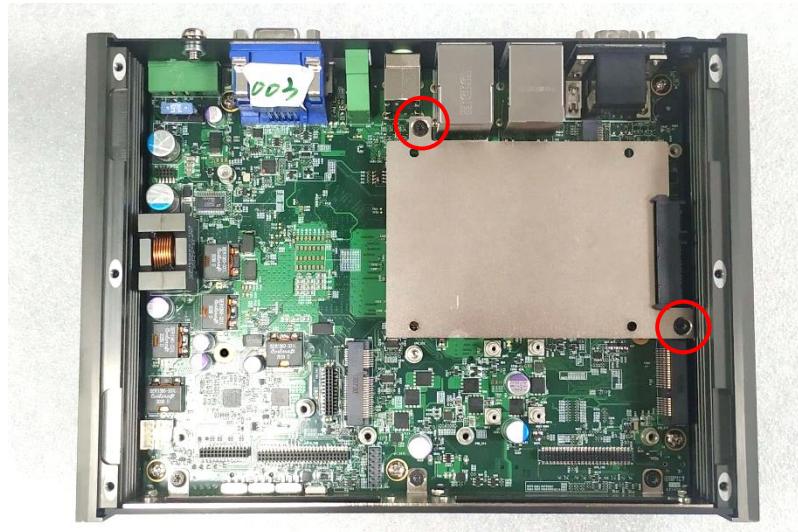
1. Turn over the unit to have the bottom side face up, loosen the 6 screws on the bottom cover and place them aside for later use.



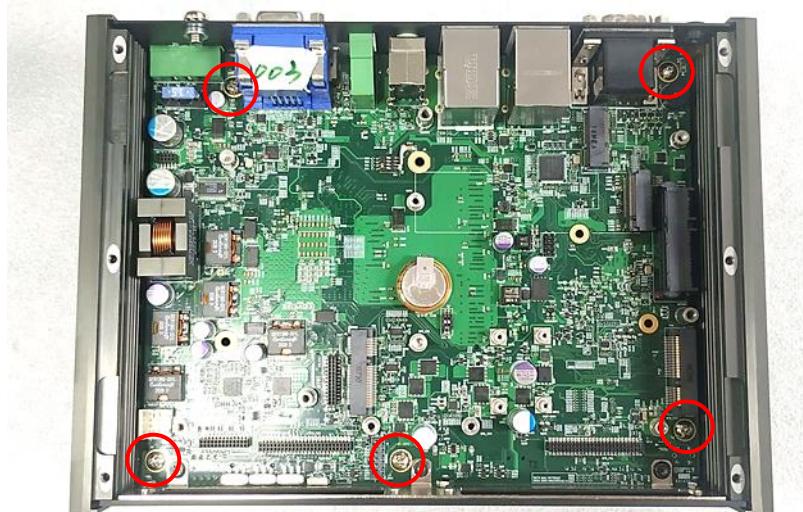
2. Remove the bottom cover from the chassis and place it aside.



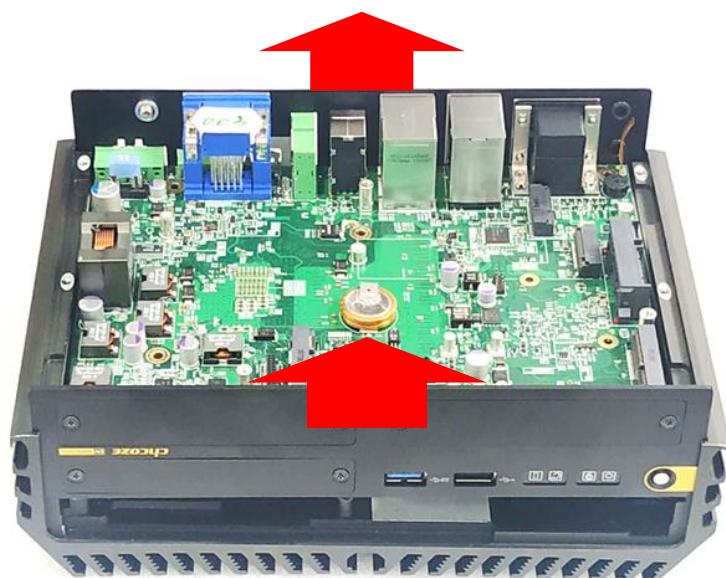
3. Loosen the indicated 2 screws and remove the HDD bracket.



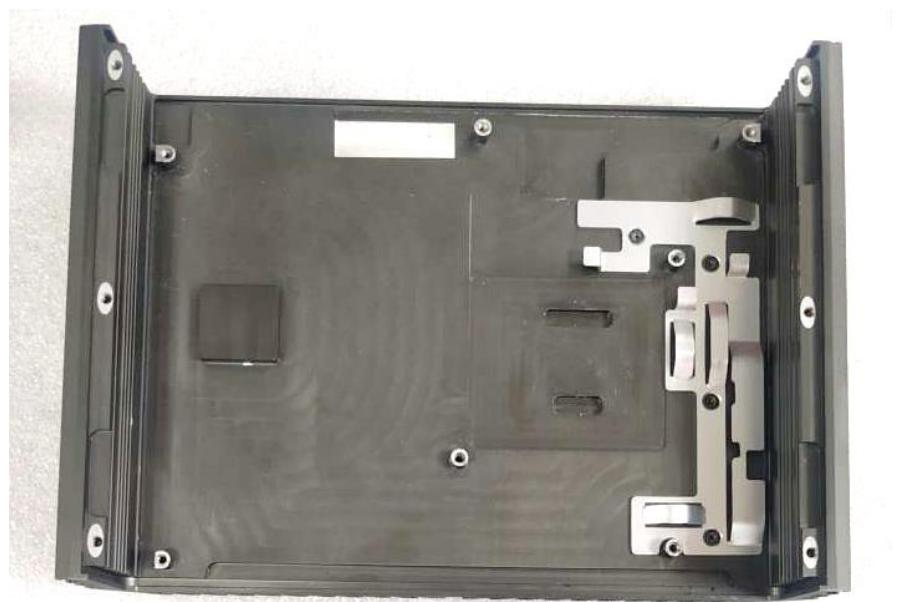
4. Loosen the indicated 5 screws



5. Hold front and rear panel and lift up the body of unit vertically.

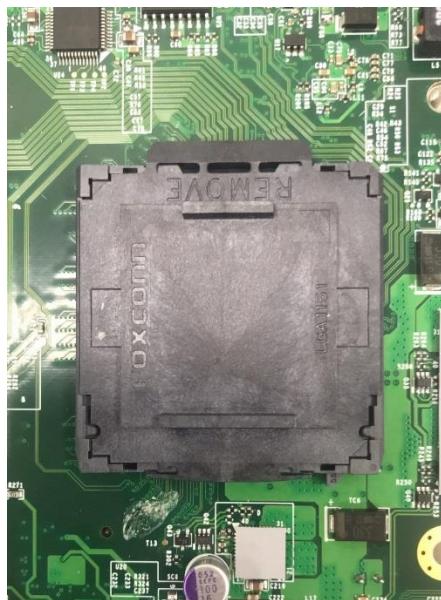


6. Turn over the body of the unit and place it gently.



## 3.2 Installing the CPU

1. Locate the CPU socket and remove the cover.



2. Insert the CPU gently by aligning the notches of the socket.



3. Place the protection cover back and fasten the two screws as indicated.



**NOTE** This holder needs a total of four screws to complete the locking. For the locking steps of the other two, please refer to the chapter of Installing Top Cover.



4. Place the thermal pad on the CPU.

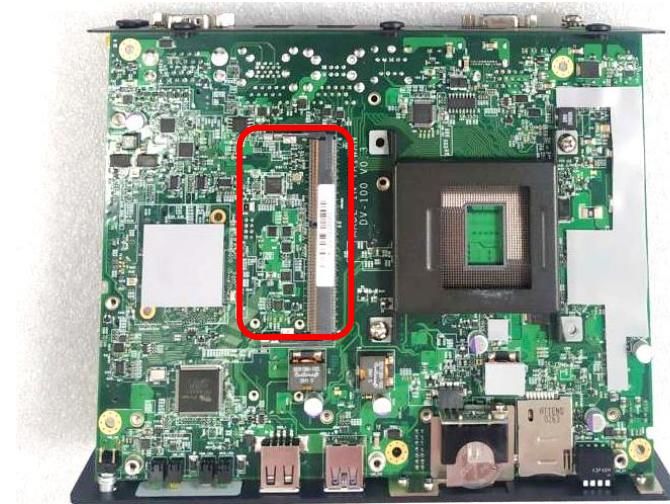


CAUTION

**Make sure the protective film on the Thermal Pad has been removed before assembling the unit back to the cover!**

### 3.3 Installing SO-DIMM

1. Locate the SODIMM socket on the top side of system.



2. Insert a SO-DIMM at a 45-degree angle until its edge connector is connected to SO-DIMM socket firmly.

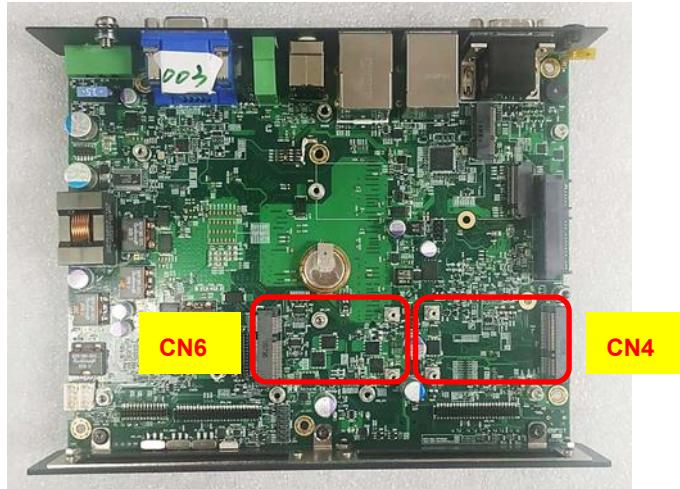


3. Press down the module until the retaining clips snap back in place.

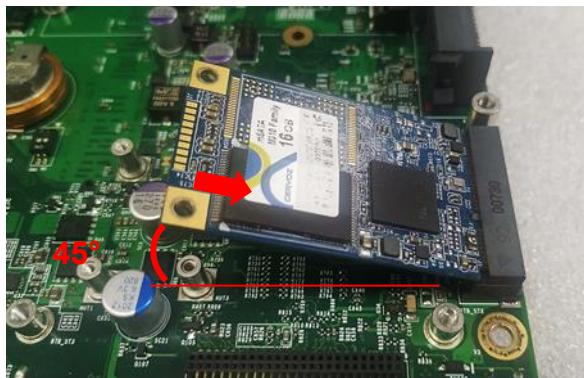


### 3.4 Installing a Mini-PCIe/mSATA Card

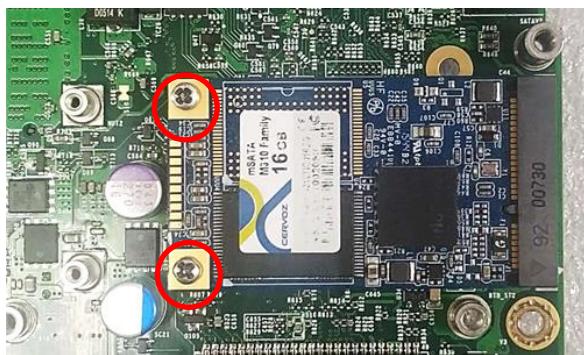
1. Locate the Mini PCIe socket(s) on the system's bottom side.



2. Insert a Mini-PCIe or mSATA card at a 45-degree angle until its edge connector is connected firmly into slot. For 3G/4G Mini-PCIe card, please install onto CN6 slot.



3. Press the card down and secure it with 2 screws.



### 3.5 Installing M.2 E Key Card

1. Locate the M.2 E Key slot (CN5) on the system motherboard.



2. Tilt the M.2 E Key card at a 45-degree angle and insert it to the socket until the golden finger connector of the card seated firmly.



3. Press the card down and secure it with 1 screw.



### 3.6 Installing M.2 M Key Card

1. Locate the M.2 M Key slot (CN7) on the system motherboard.



2. Tilt the M.2 M Key card at a 45-degree angle and insert it to the socket until the golden finger connector of the card seated firmly.



3. Press the card down and secure it with the screw.



## 3.7 Installing Antennas



NOTE

Please install a Mini PCIe wireless LAN card at MINI PCIe socket before antenna installation.

1. Remove the antenna plug on the rear panel.



2. Penetrate the antenna jack through the hole.



3. Put on the washer and fasten the nut of antenna jack.



4. Assemble the antenna and antenna jack together.

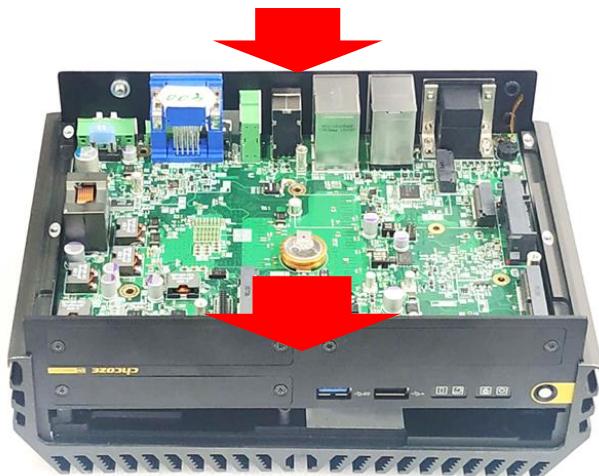


5. Attach the RF connector of the cable's another end onto the card.

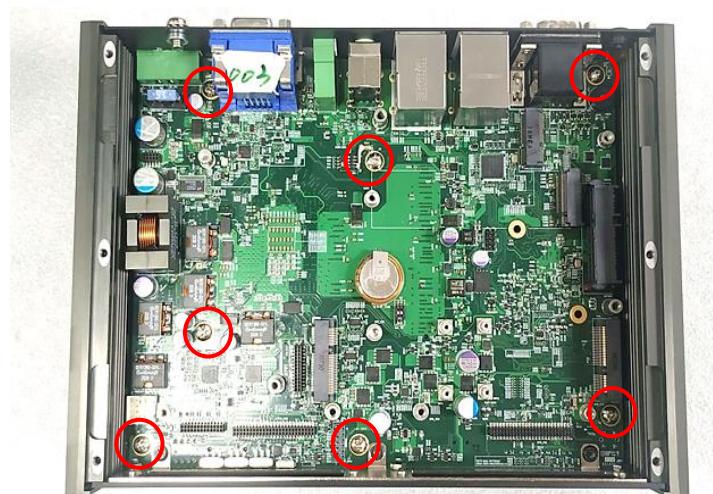


## 3.8 Installing Top Cover

1. Hold front and rear panel and put the body of unit back to chassis.

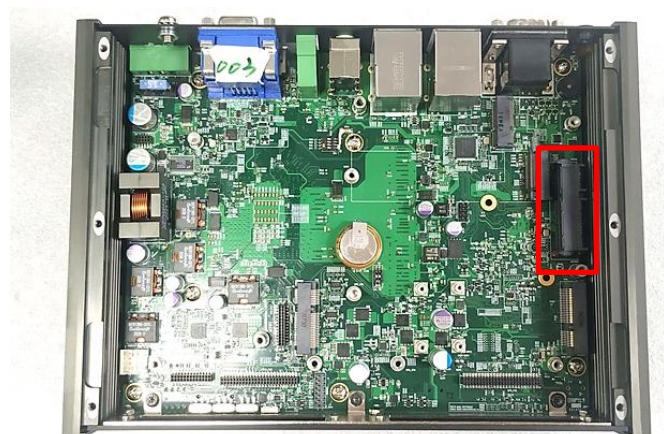


2. Fasten the indicated 7 screws

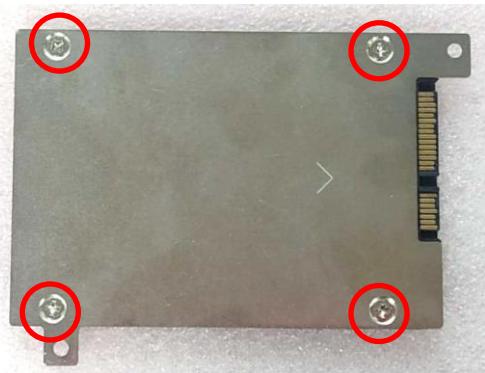


## 3.9 Installing SATA Hard Drive

1. Locate the HDD slot.



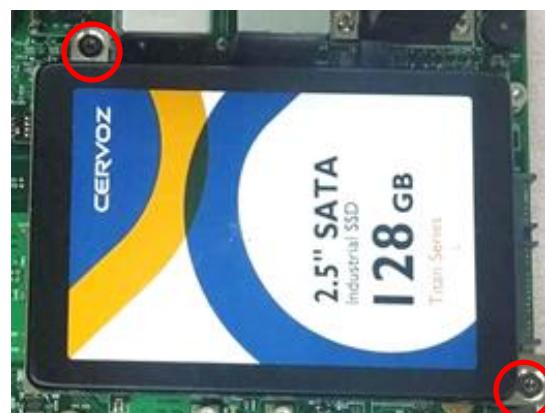
2. Make HDD bottom side face up, place the HDD bracket on it. Ensure the direction of bracket is correct and use 4 provided screws to assemble HDD and HDD bracket together.



3. Insert the HDD bracket and push it until the HDD connector is fully inserted into the SATA slot.

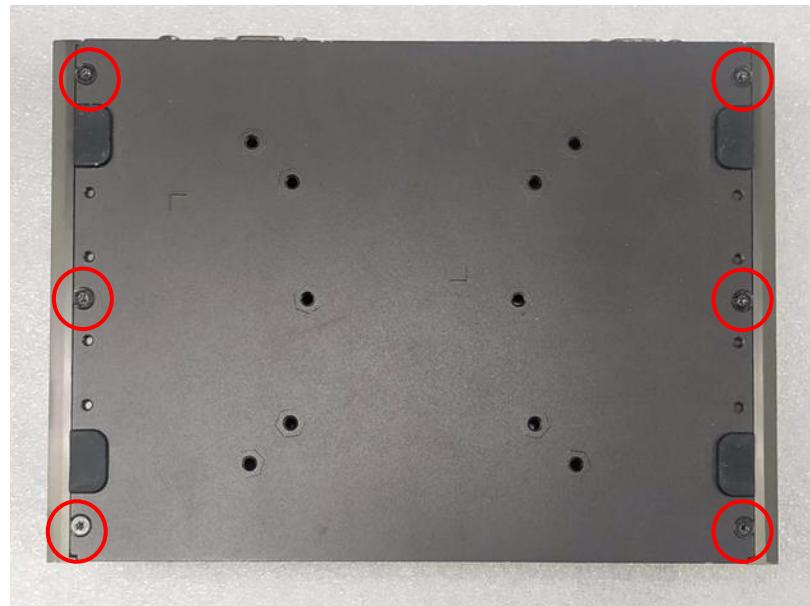


4. Fix the HDD bracket by fastening the two screws.



## 3.10 Installing Bottom Cover

1. Place the bottom cover back to system and fasten it with the 6 screws.



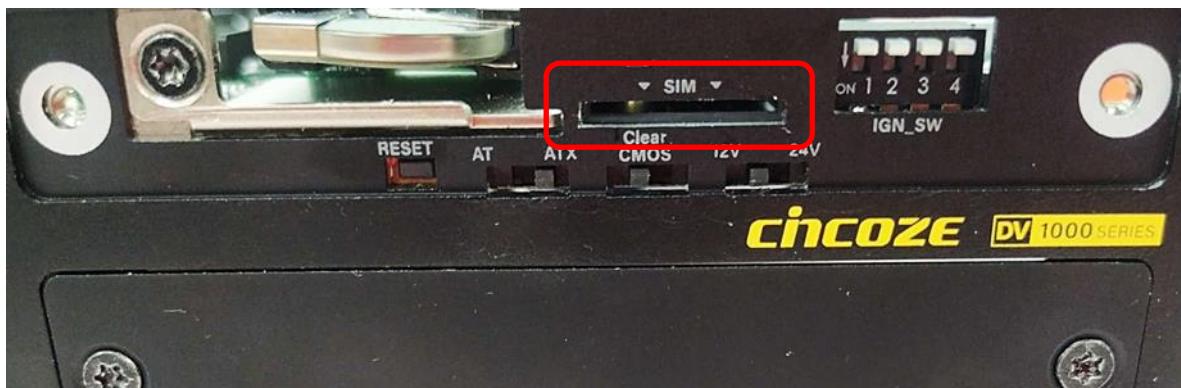
## 3.11 Removing the Front Cover Plate

1. Loosen the 2 screws on the front cover plate and remove it.



### 3.12 Installing a SIM Card

1. Locate the SIM card slot at front side.



2. Insert a SIM card into SIM slot with the gold contacts facing up. Please pay attention to the insert orientation as illustrated.



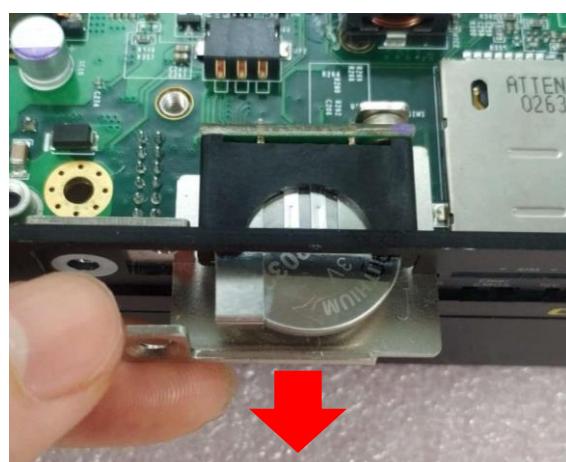
### 3.13 Replacing the CMOS Battery

This chapter is to introduce how to replace the CMOS battery when it is dead.

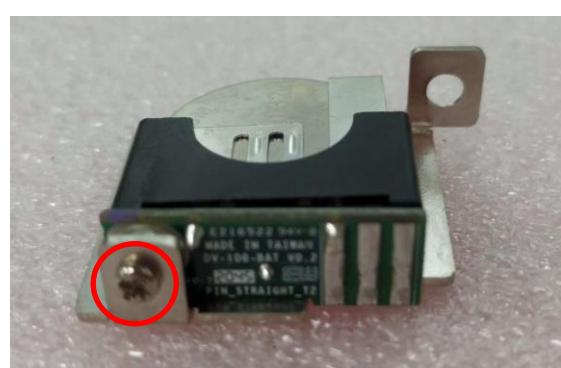
1. Locate the removable CMOS Battery and loosen the screw.



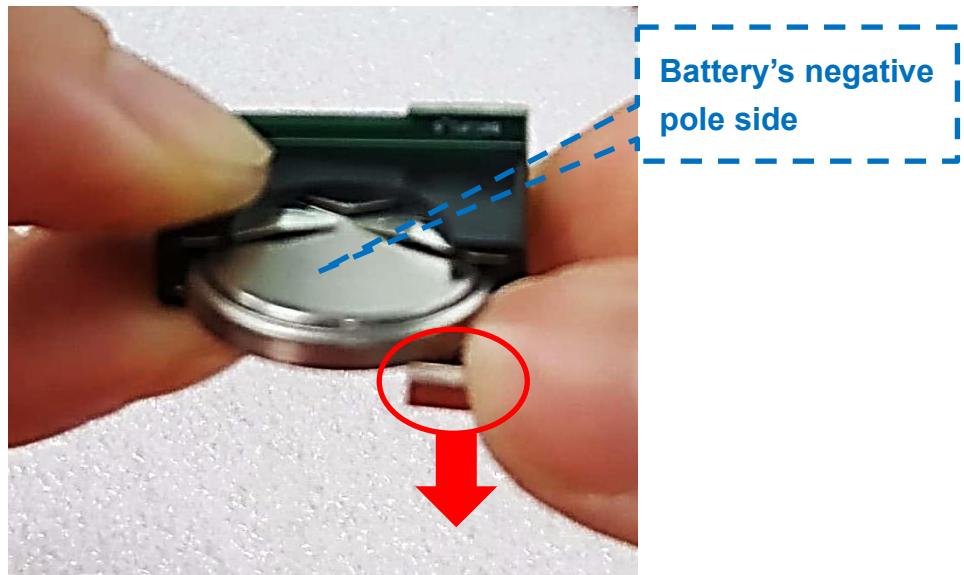
2. Pull out the CMOS battery bracket.



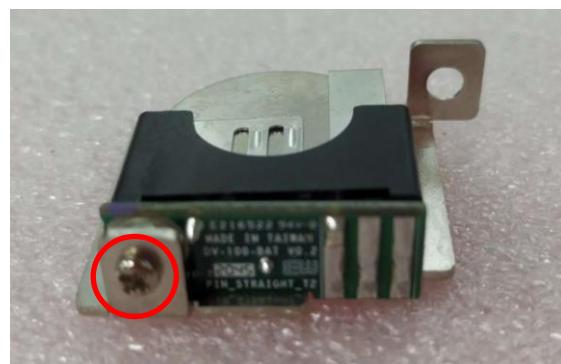
3. Loosen the screw.



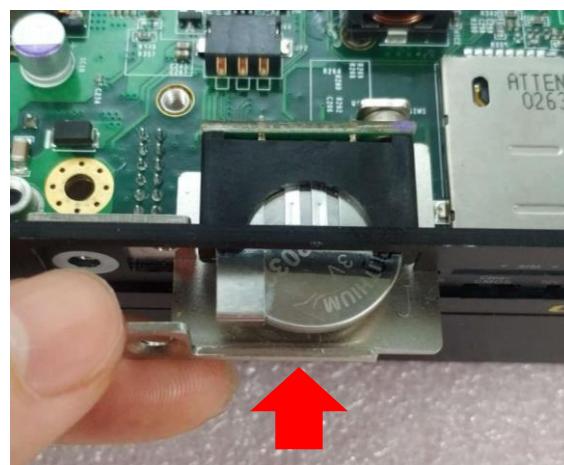
4. Pull down the indicated portion and replace the CMOS battery with a new one. (please note the battery's positive/negative pole orientation when you execute this step).



5. Fasten the screw back.



6. Insert the CMOS battery bracket.



7. Fasten the screw back.



### 3.14 Fastening the Cover

1. Fasten the cover by using the two screws.

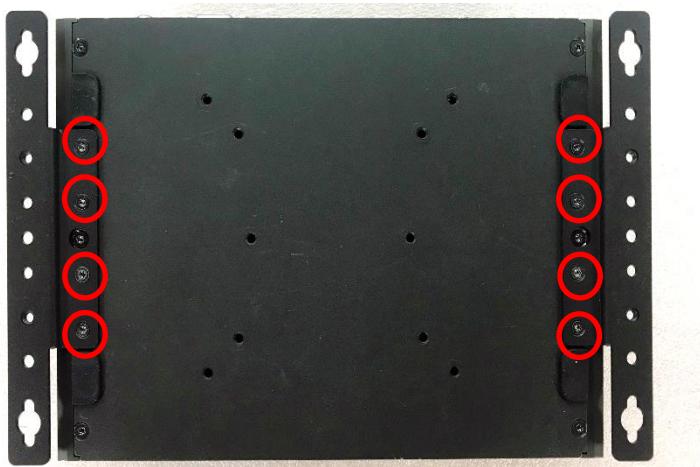


### **3.15 Wall Mount Brackets**

This system offers wall mount brackets for customers to install system on the wall in a convenient and economical way.



1. The mounting holes are at the bottom side of system. Use provided 8 screws to fasten the bracket on each side.

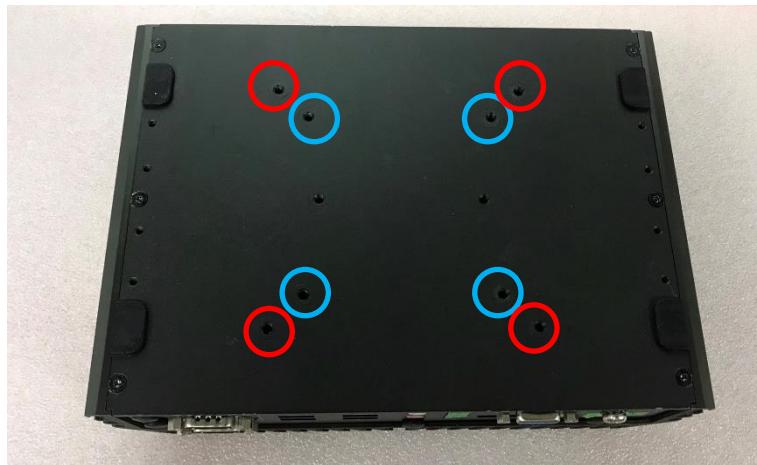


2. There are 2 mounting holes at each wall mount bracket for user to fix the system onto the wall.



### **3.16 VESA Mount**

This system supports VESA mounting that customer can mount it onto VESA stand for various usage. The blue-circle-marked screw holes support the 75mm standard of the VESA stand. The red-circle-marked screw holes support the 100mm standard of the VESA stand.



1. The following picture illustrates the installation of the system on a VESA stand. Align the 4 screw holes of VESA stand with the screw holes on bottom side of system. Fasten the 4 screws to fix it.



2. Provided below is the completion of mounting with the VESA stand.



# **Chapter 4**

## **BIOS Setup**

## 4.1 BIOS Introduction

The BIOS (Basic Input/ Output System) is a program located on a Flash Memory on the motherboard. When you start the computer, the BIOS program will gain control. The BIOS first operates an auto-diagnostic test called POST (power on self-test) for all the necessary hardware, it detects the entire hardware device and configures the parameters of the hardware synchronization.

### BIOS Setup

Power on the computer and by pressing <Del> immediately allows you to enter Setup. If the message disappears before your respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing <Ctrl>, <Alt> and <Delete> keys.

Control Keys	
<--> <-->	Move to select screen
<↑> <↓>	Move to select item
<Esc>	Quit the BIOS Setup
<Enter>	Select item
<Page Up/+>	Increases the numeric value or makes changes
<Page Down/->	Decreases the numeric value or makes changes
<Tab>	Select setup fields
<F1>	General help
<F2>	Previous value
<F3>	Load Optimized defaults
<F10>	Save configuration and Exit

### Main Menu

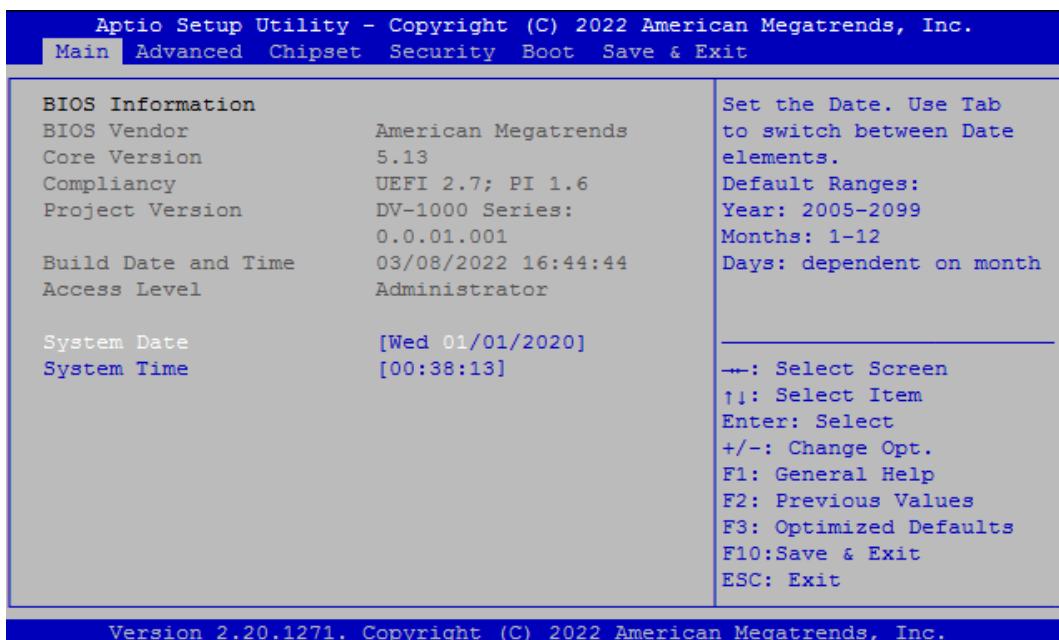
The main menu lists the setup functions you can make changes to. You can use the arrow keys ( ↑ ↓ ) to select the item. The on-line description of the highlighted setup function is displayed at the bottom of the screen.

### Sub-Menu

If you find a right pointer symbol appears to the left of certain fields that means a sub-menu can be launched from this field. A sub-menu contains additional options for a field parameter. You can use arrow keys ( ↑ ↓ ) to highlight the field and press <Enter> to call up the sub-menu. Then you can use the control keys to enter values and move from field to field within a sub-menu. If you want to return to the main menu, just press the <Esc >.

## 4.2 Main Setup

Press <Del> to enter BIOS CMOS Setup Utility, the Main Menu (as shown below) will appears on the screen. Use arrow keys to move among the items and press <Enter> to accept or enter a sub-menu.



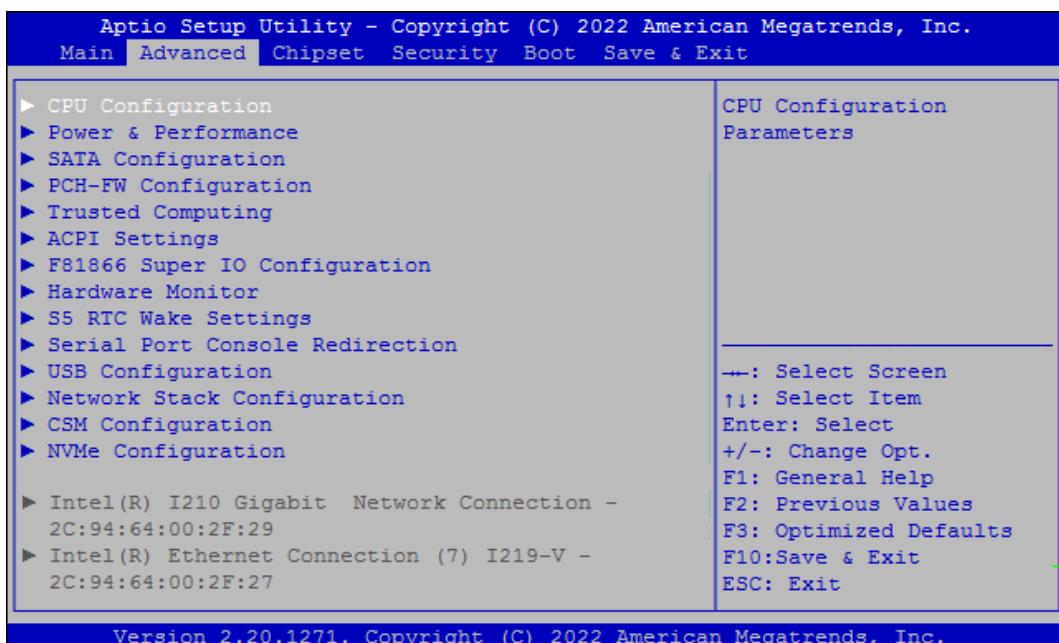
### 4.2.1 System Date

Set the date. Please use <Tab> to switch between date elements.

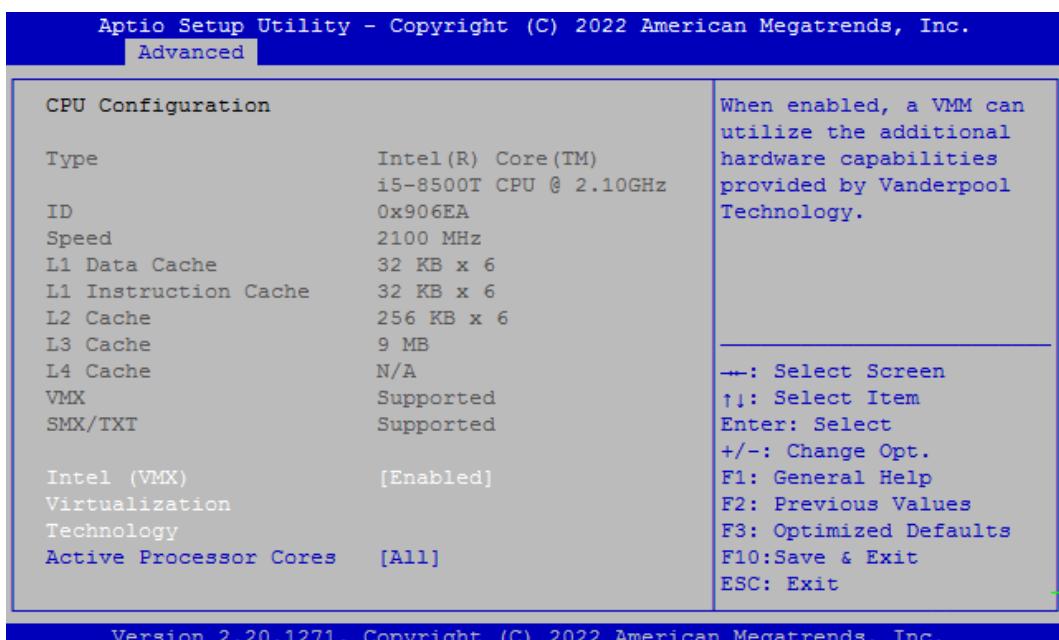
### 4.2.2 System Time

Set the time. Please use <Tab> to switch between time elements.

## 4.3 Advanced Setup



### 4.3.1 CPU Configuration



### ■ Intel® (VXM) Virtualization Technology

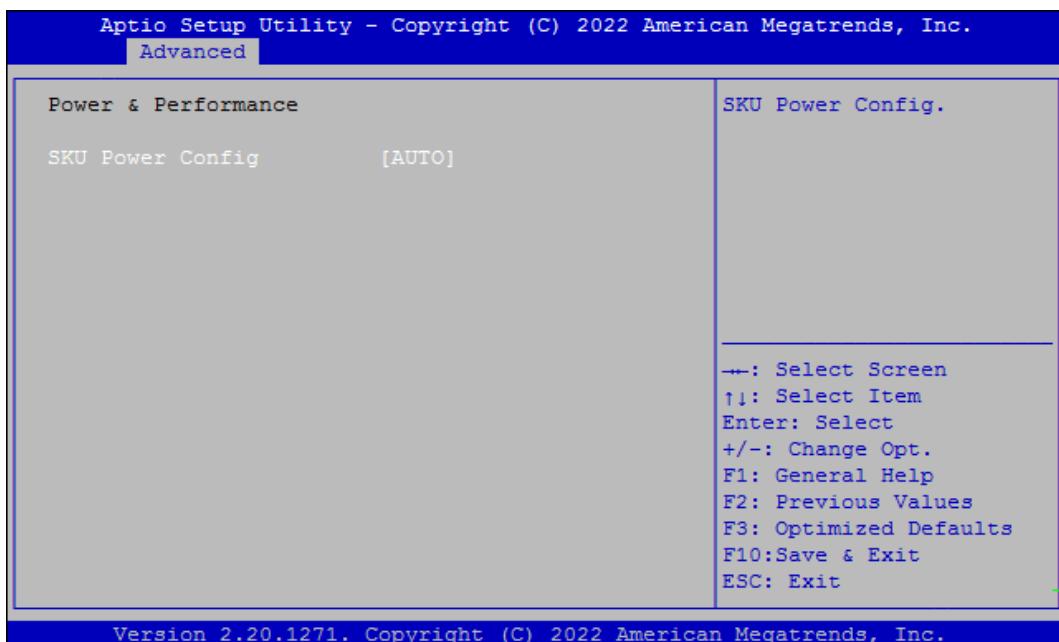
Enables or disables Intel® Virtualization Technology, which will allow a platform to run multiple operating systems and applications in independent partitions. With virtualization, one computer system can function as multiple virtual systems.

### ■ Active Process Cores

Allows you to choose the number of active processor cores.

Configuration options: [All] [1] [2] [3] [4] [5].

### 4.3.2 Power & Performance

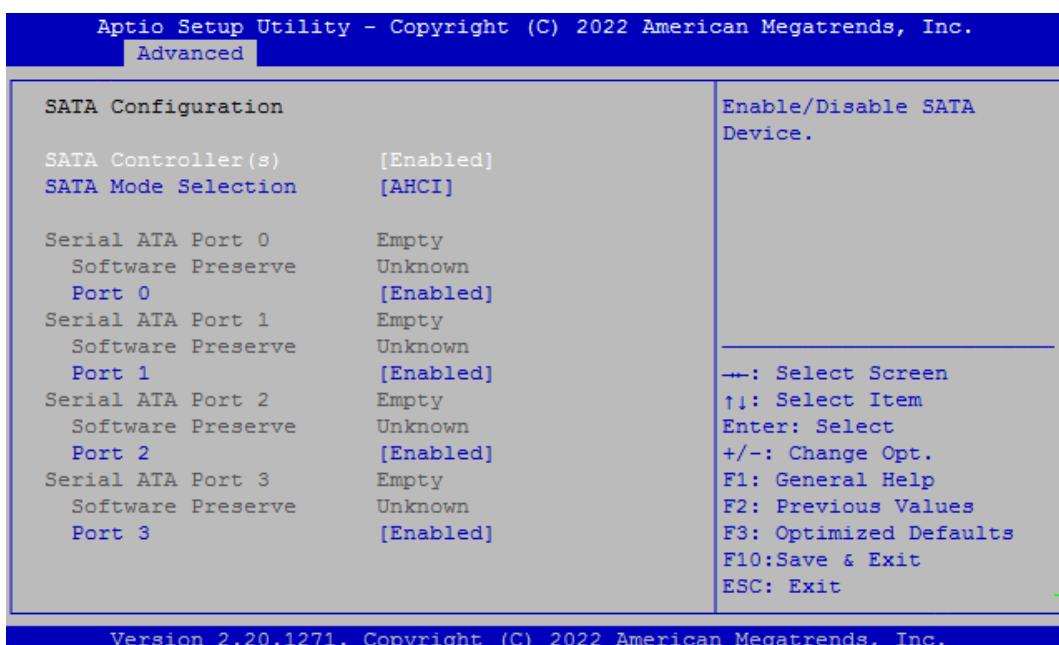


#### ■ SKU Power Config [Auto]

Allows users to choose the upper limit of CPU power.

Configuration options: [Auto] [35W]

### 4.3.3 SATA Configuration



#### ■ SATA Controller(s) [Enabled]

Enables or disables SATA device.

#### ■ SATA Mode Selection [AHCI]

Allows you to select which mode SATA controller will operate.

Configuration options: [AHCI], [RAID]

##### Serial ATA Port 0

##### Port 0 [Enabled]

Enables or disables SATA Port 0.

**Serial ATA Port 1**

**Port 1 [Enabled]**

Enables or disables SATA Port 1.

**Serial ATA Port 2**

**Port 1 [Enabled]**

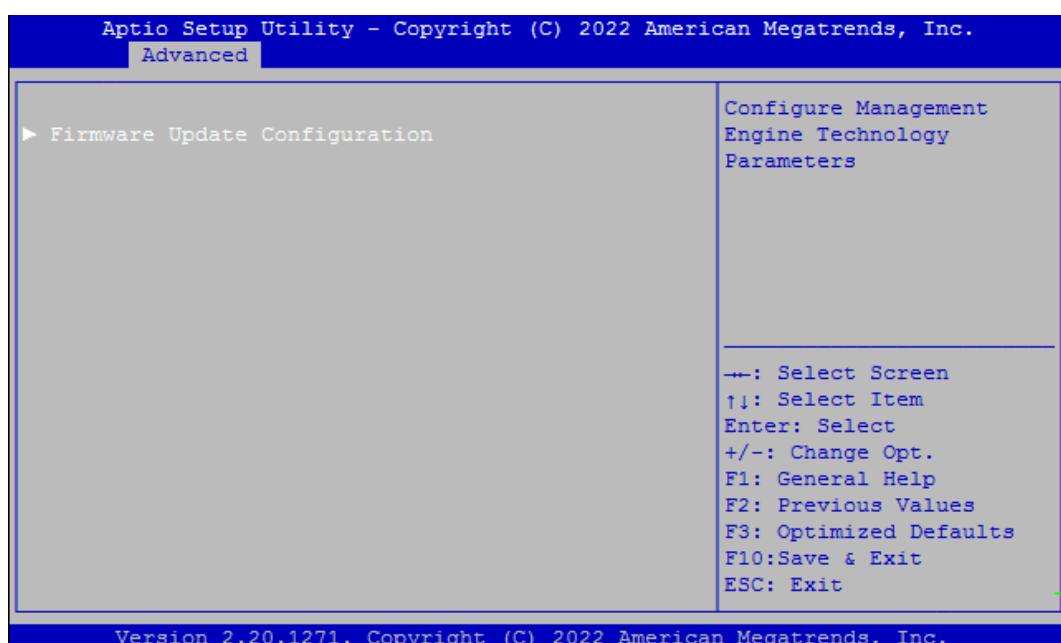
Enables or disables SATA Port 2.

**Serial ATA Port 3**

**Port 1 [Enabled]**

Enables or disables SATA Port 3.

#### 4.3.4 PCH-FW Configuration



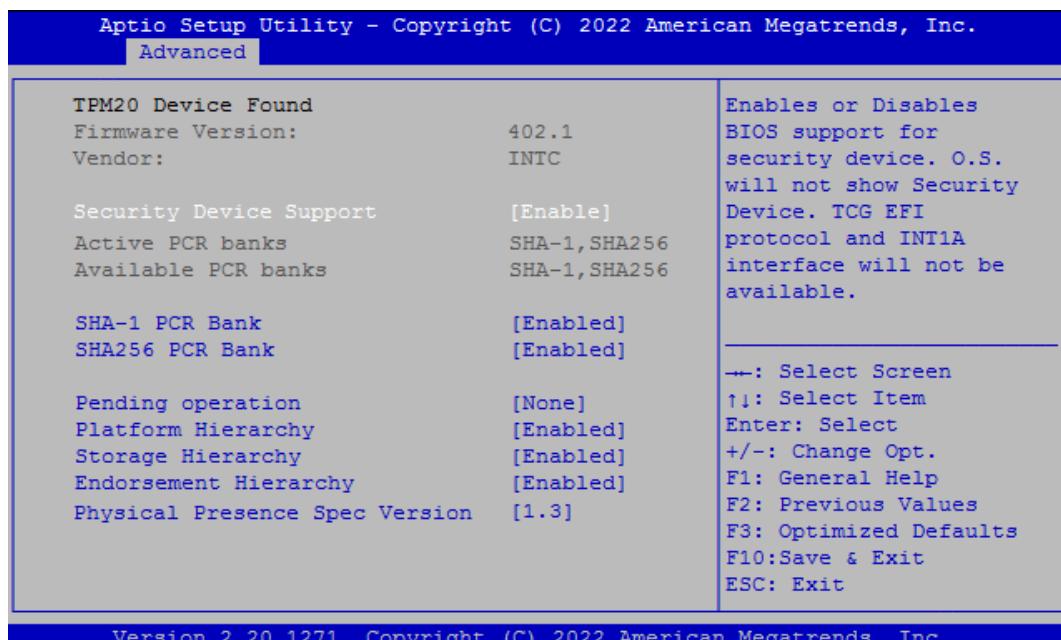
#### ■ Firmware Update Configuration

Configure Management Engine Parameters

**Me FW Image Re-Flash [Disabled]**

Enables or disables ME firmware Image Re-Flash function.

#### 4.3.5 Trusted Computing Settings



##### ■ Security Device Support [Enabled]

Enables or disables Security Device Support function.

##### ■ SHA-1 PCR Bank [Enabled]

Enables or disables SHA-1 PCR Bank function.

##### ■ SHA256 PCR Bank [Enabled]

Enables or disables SHA256 PCR Bank function.

##### ■ Pending Operation [None]

Allows you to select which mode Pending Operation will operate.

Configuration options: [None], [TPM Clear]

##### ■ Platform Hierarchy [Enabled]

Enables or disables Platform Hierarchy function.

##### ■ Storage Hierarchy [Enabled]

Enables or disables Storage Hierarchy function.

##### ■ Endorsement Hierarchy [Enabled]

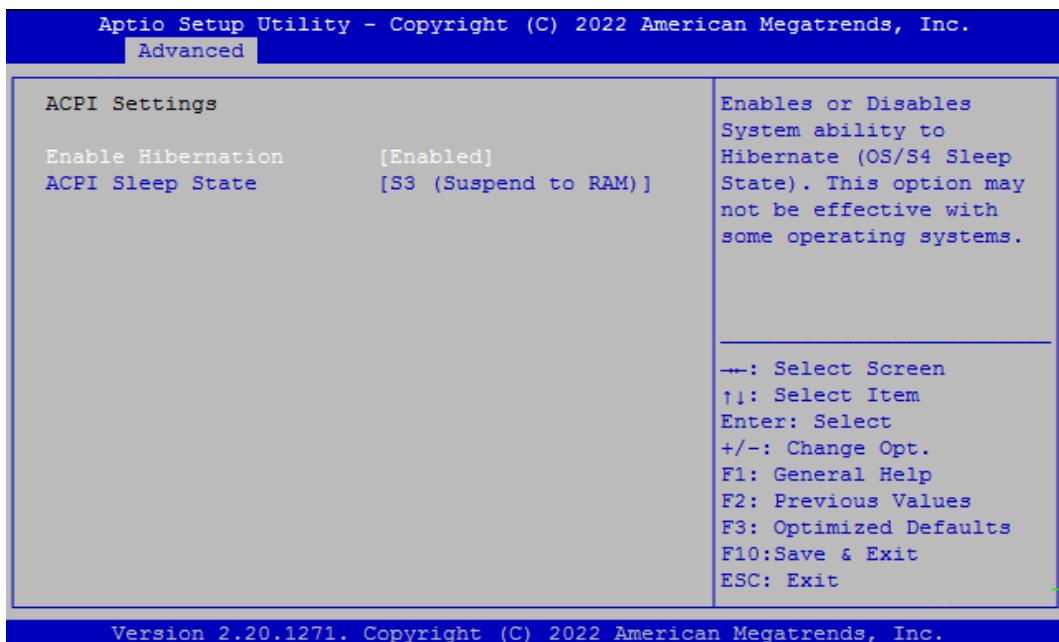
Enables or disables Endorsement Hierarchy function.

##### ■ Physical Presence Spec Version [1.3]

Allows you to select which mode Physical Presence Spec Version will operate.

Configuration options: [1.2], [1.3]

#### 4.3.6 ACPI Settings



##### ■ Enable Hibernation [Enabled]

Enables or disables system ability to hibernate state (OS/S4 state). This option may not be effective with some OS.

##### ■ ACPI Sleep State [S3 (Suspend to RAM)]

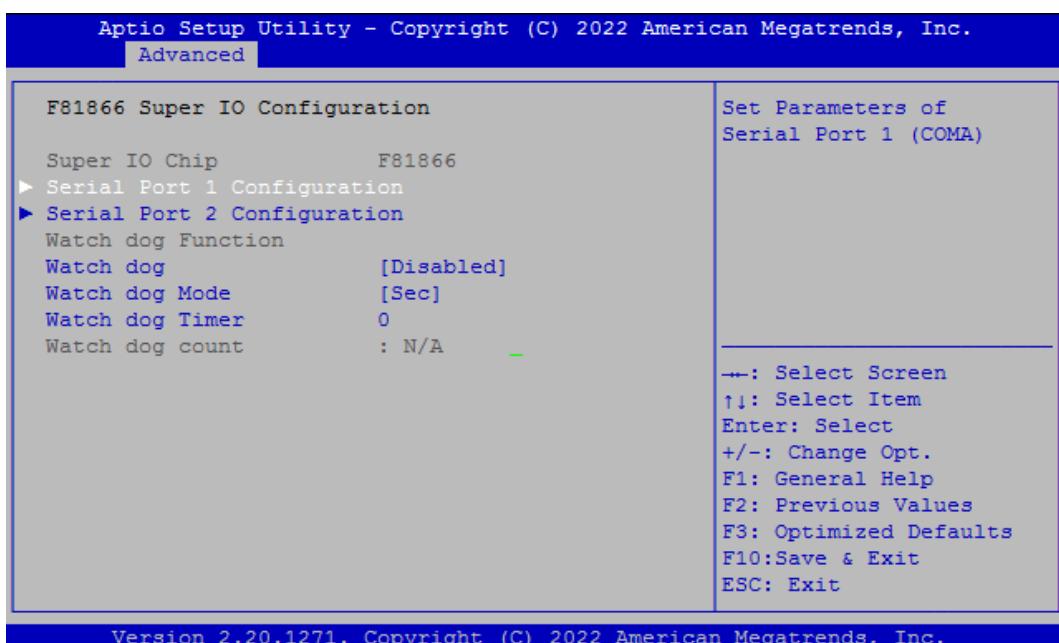
Allows users to select the highest Advanced Configuration Power Interface® (ACPI) sleep state that system will enter when suspend button is pressed.

[Suspend Disabled]: Disables entering suspend state.

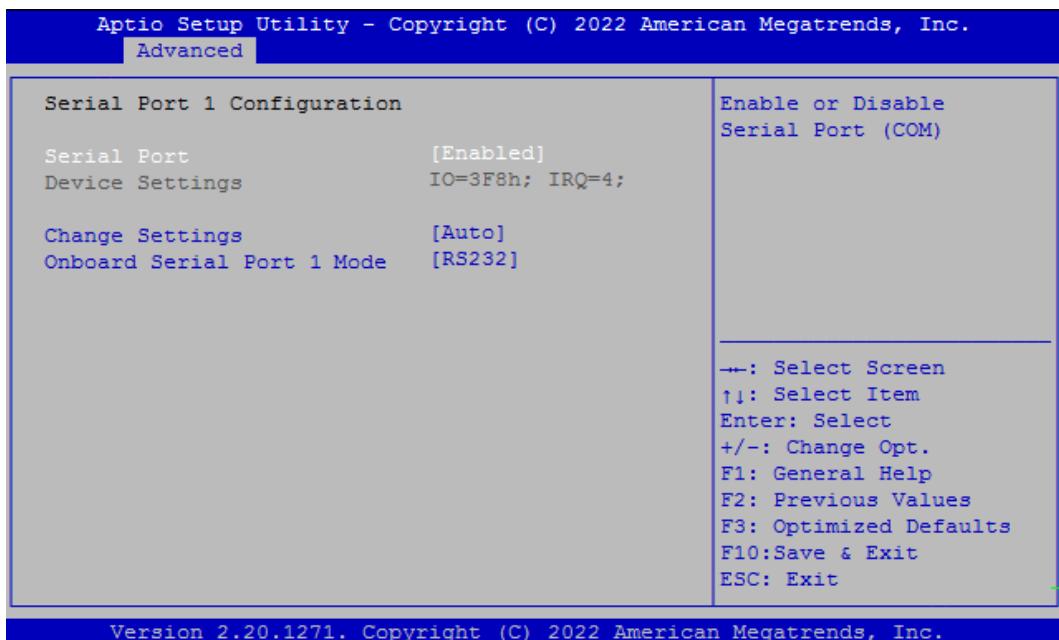
[S3 (suspend to RAM)]: Enables suspend to RAM state.

#### 4.3.7 F81866 Super IO Configuration

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal setting for the Super IO Device.



## ■ Serial Port 1~2 Configuration.



### **Serial Port [Enabled]**

Enables or disables serial port.

### **Change Settings [Auto]**

Allows you to change the IO Address & IRQ settings of the specified serial port.

### **Onboard Serial Port 1~2 Mode [RS232]**

Allows you to select Serial Port Mode.

Configuration options: [RS232] [RS422/RS485 Full Duplex] [RS485 Half Duplex]

## ■ Watch Dog [Disabled]

Enables or disables watch dog function.

## ■ Watch Dog Mode [Sec]

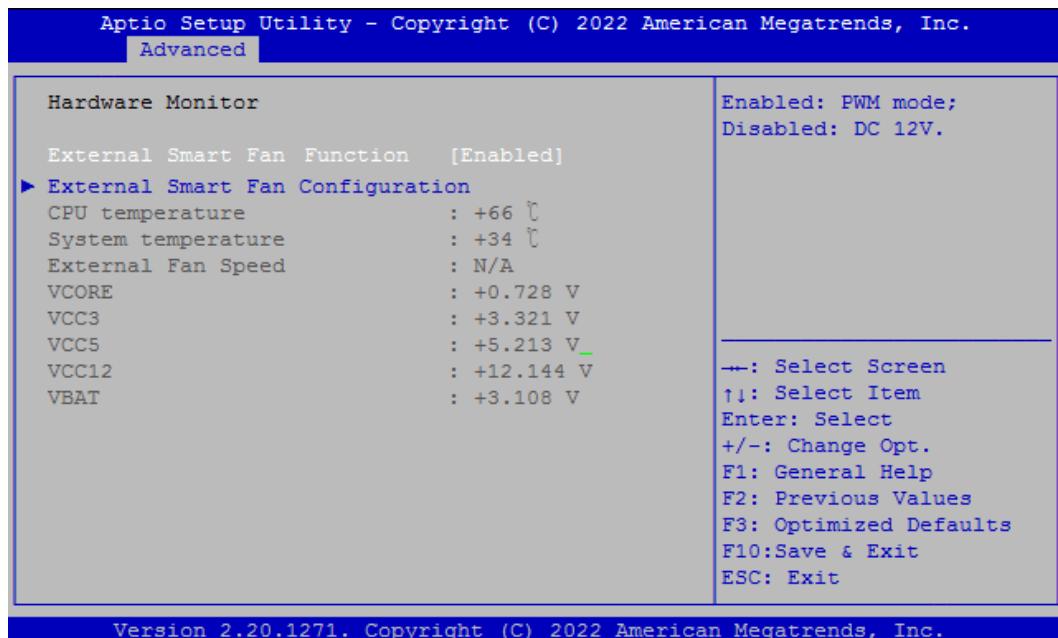
Allows to set watchdog timer unit <Sec> or <Min>.

## ■ Watch Dog Timer [0]

Allows you to set watchdog timer's value in the range of 0 to 255.

#### 4.3.8 Hardware Monitor

This screen displays the current status of all monitored hardware devices/components such as voltages, temperatures and all fans' speeds.

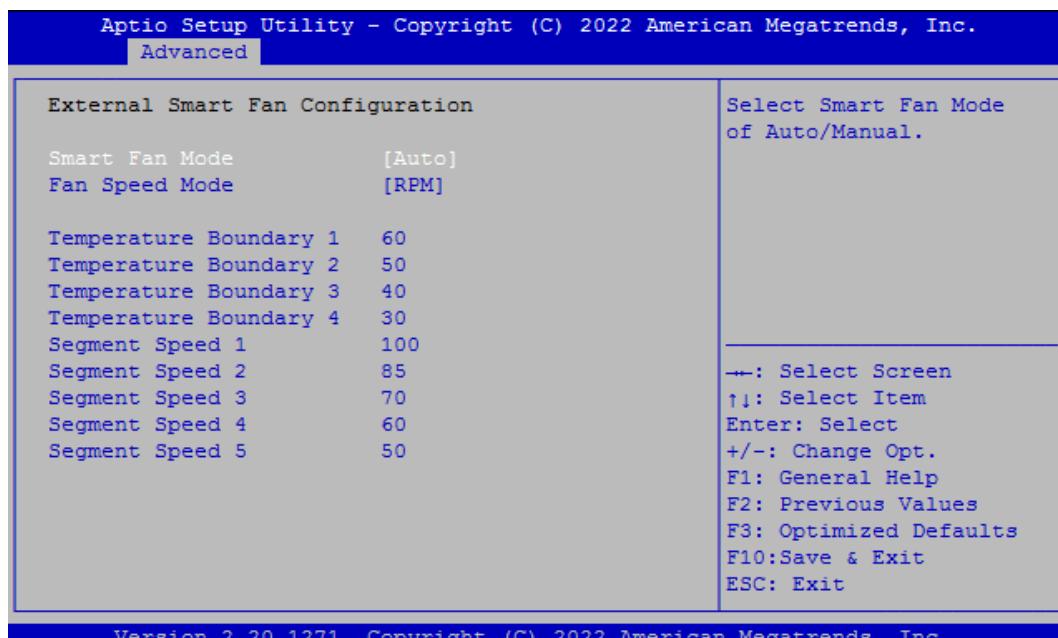


#### ■ External Smart Fan Function [Enabled]

Enables or disables External Smart Fan function.

#### ■ External Smart Fan Configuration

Configure External Smart Fan Parameters.



#### □ Smart Fan Mode [Auto]

Allows you to select Smart Fan Mode.

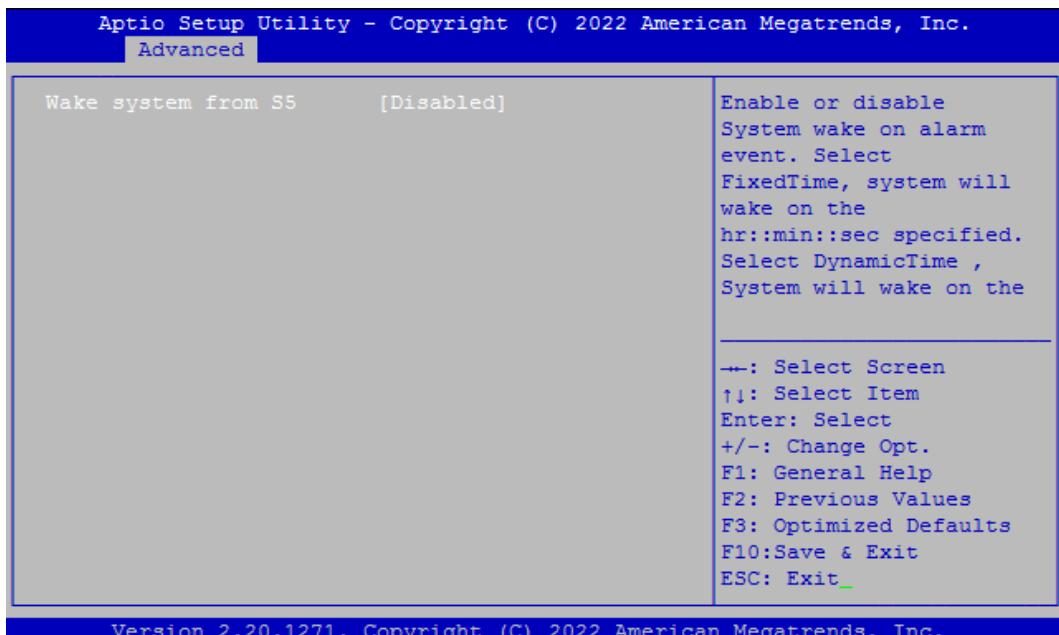
Configuration options: [Auto] [Manual]

#### □ Fan Speed Mode [RPM]

Allows you to select Fan Speed Mode.

Configuration options: [RPM] [Duty]

#### 4.3.9 S5 RTC Wake Settings



##### ■ Wake system from S5 [Disabled]

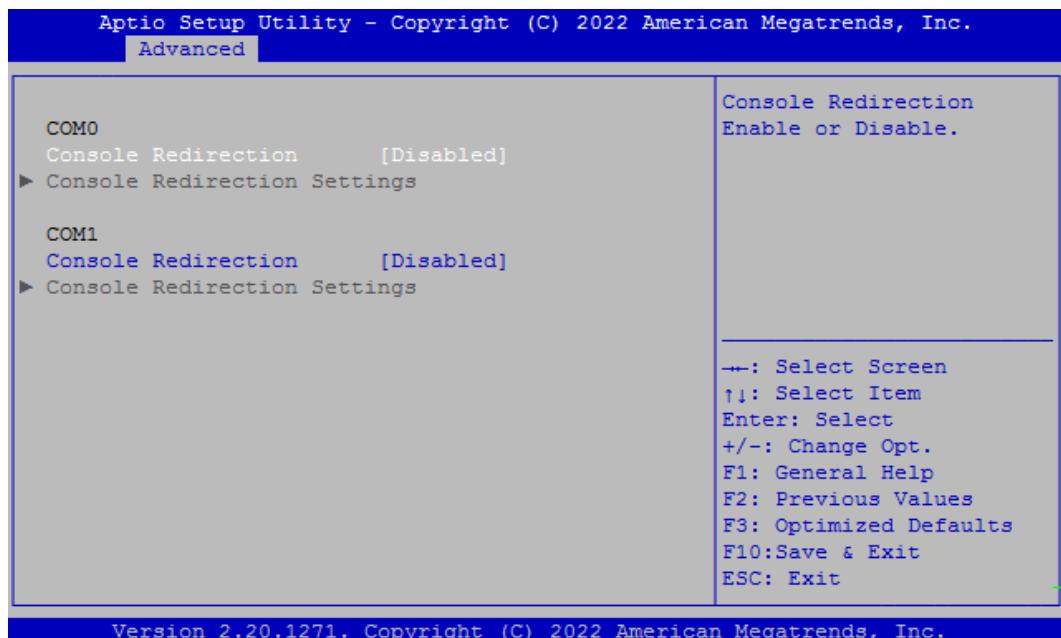
Enables or disables wake system from S5 (soft-off state).

[Disabled]: Disables wake system from S5.

[Fixed Time]: Sets a fixed time (HH:MM:SS) to wake system from S5.

[Dynamic Time]: Sets an increase minute(s) from current time to wake system from S5.

#### 4.3.10 Serial Port Console Redirection



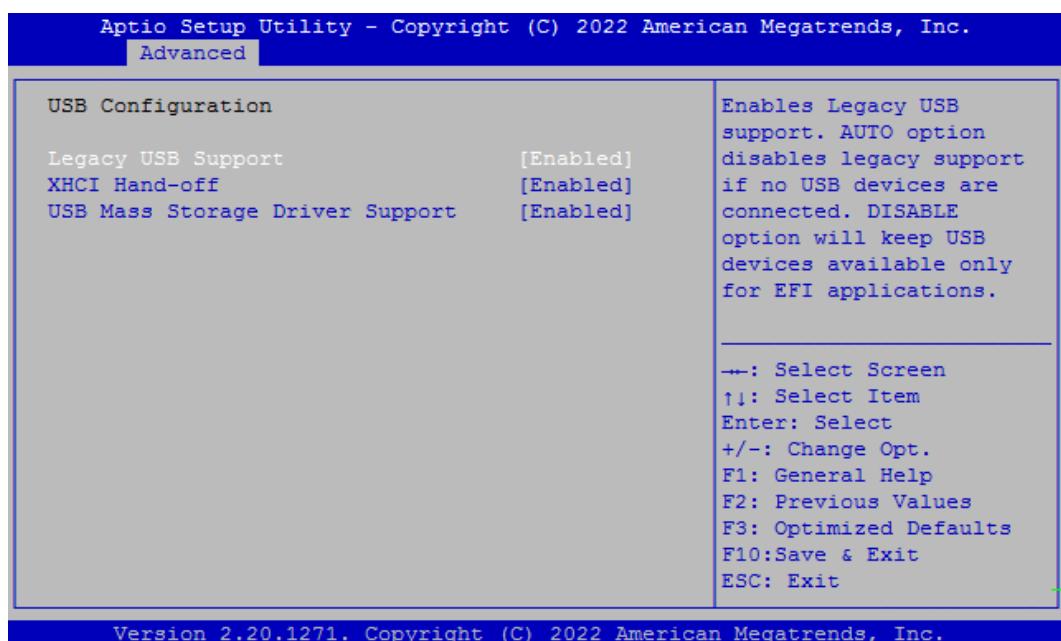
#### ■ Console Redirection

Allow users to enable or disable COM0, COM1 console redirection function.

COM0 = Serial Port 1

COM1 = Serial Port 2

#### 4.3.11 USB Configuration



### ■ Legacy USB Support [Enabled]

This item allows you to enable or disable legacy USB support. When set to [Auto], legacy USB support will be disabled automatically if no USB devices are connected.

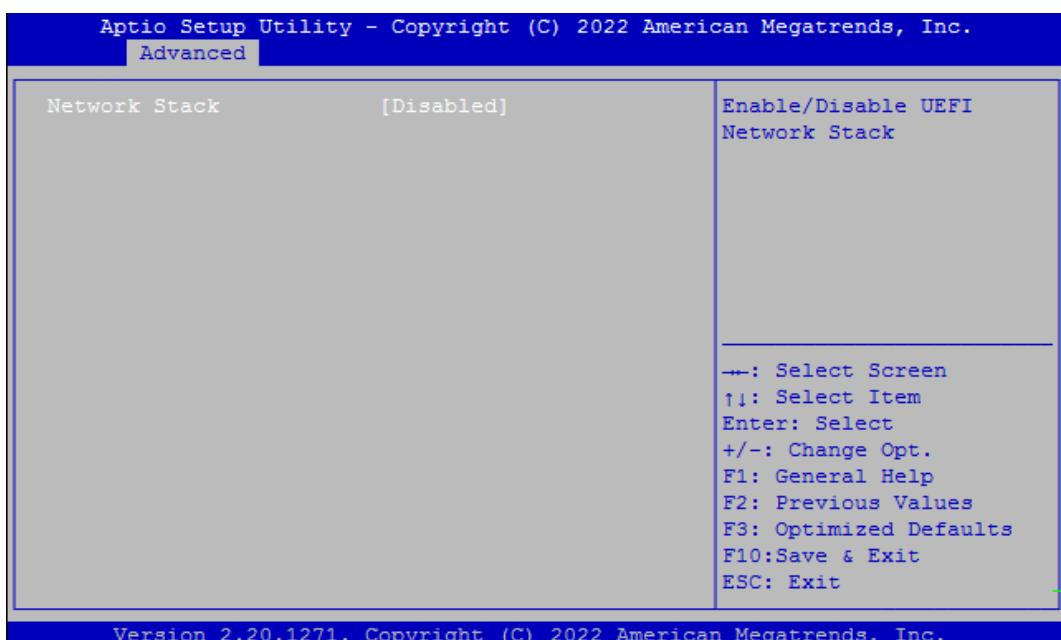
### ■ XHCI Hand-off [Enabled]

Enables or disables XHCI (USB3.0) hand-off function. Use this feature as a workaround for operating systems without XHCI hand-off support.

### ■ USB Mass Storage Driver Support [Enabled]

Enables or disables USB mass storage driver support.

## 4.3.12 Network Stack Configuration

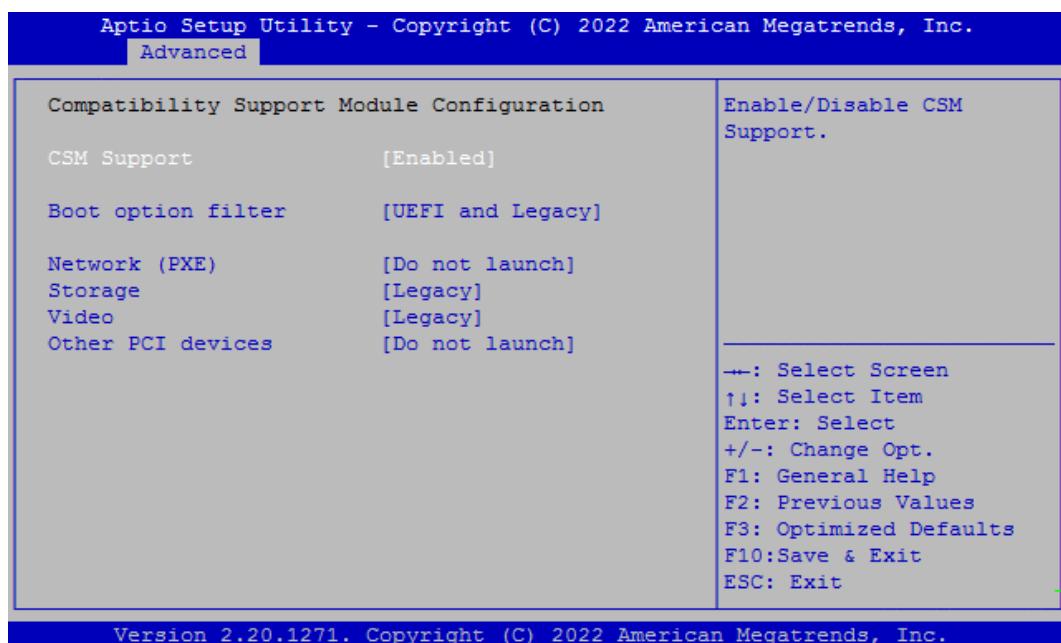


### ■ Network Stack [Disabled]

Enables or disables UEFI Network Stack.

### 4.3.13 CSM Configuration

This option controls legacy/UEFI ROMs priority.



#### ■ CSM Support [Enabled]

Enables or disables compatibility support module.

#### ■ Boot option filter [UEFI and Legacy]

Allows you to select which type of operating system to boot.

[UEFI and Legacy]: Allows booting from operating systems that support legacy option ROM or UEFI option ROM.

[Legacy only]: Allows booting from operating systems that only support legacy option ROM.

[UEFI only]: Allows booting from operating systems that only support UEFI option ROM.

#### ■ Network PXE [Do not launch]

Controls the execution of UEFI and Legacy PXE (Network Preboot eXecution Environment) option ROM.

[Do not launch]: Disables option ROM execution.

[UEFI]: Enables UEFI option ROM only.

[Legacy]: Enables legacy option ROM only.

#### ■ Storage [Legacy]

Controls the execution of UEFI and Legacy Storage option ROM.

[Do not launch]: Disables option ROM execution.

[UEFI]: Enables UEFI option ROM only.

[Legacy]: Enables legacy option ROM only.

#### ■ Video [Legacy]

Controls the execution of UEFI and Legacy Video option ROM.

[Do not launch]: Disables option ROM execution.

[UEFI]: Enables UEFI option ROM only.

[Legacy]: Enables legacy option ROM only.

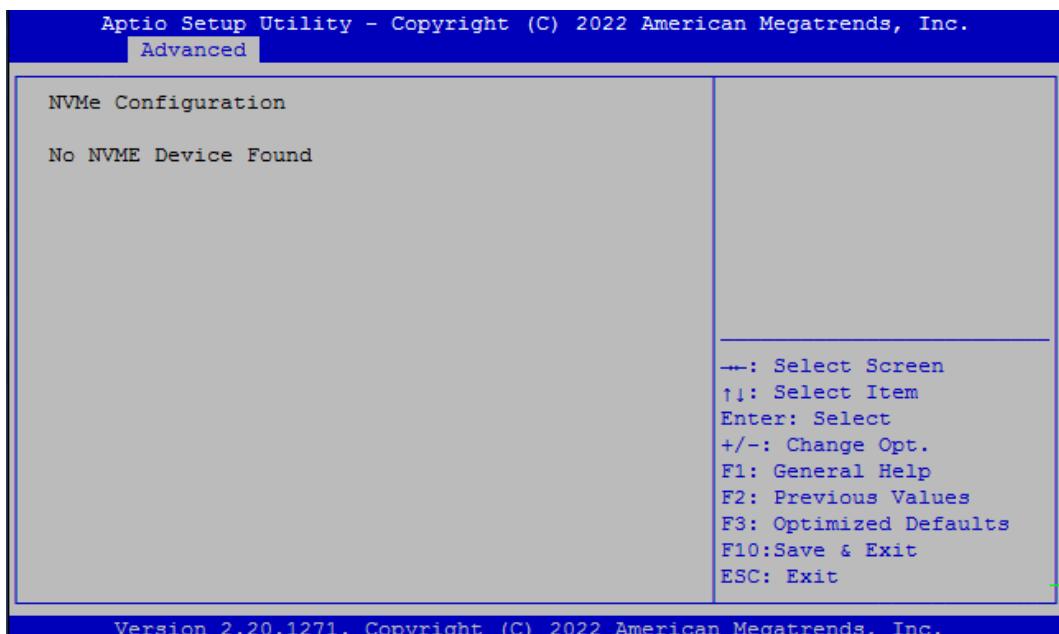
## ■ Other PCI devices [Do not launch]

Allows users to determine option ROM execution policy for device other than network, storage, or video.

Configuration options: [Do not launch] [UEFI] [Legacy]

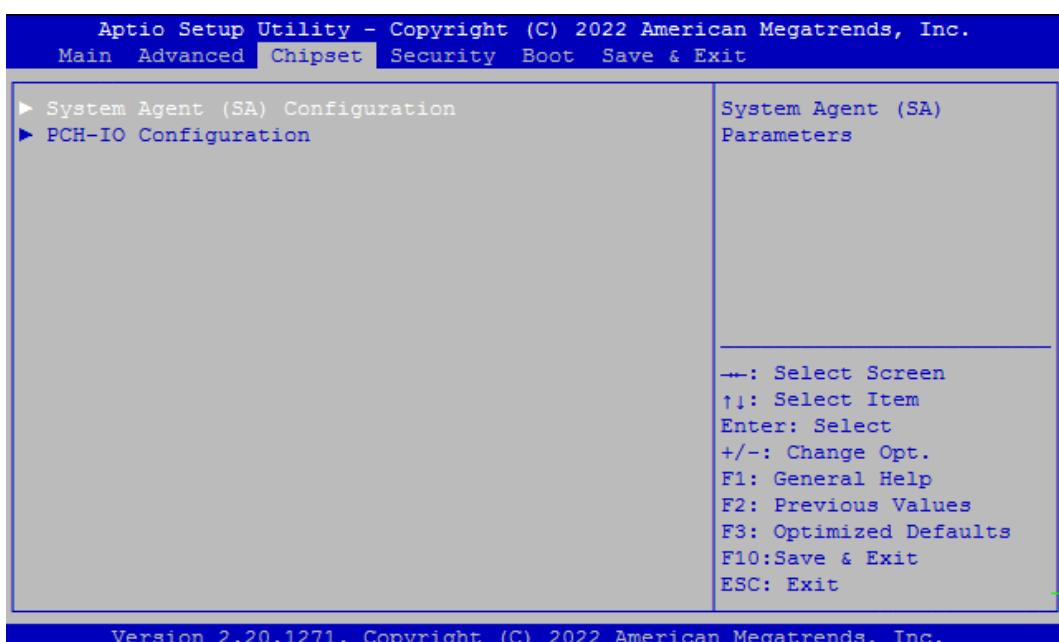
### 4.3.14 NVMe Configuration

The screen allows users to select options for the NVMe configuration, and change the value of the selected option. The options will show as the NVME Device is found.

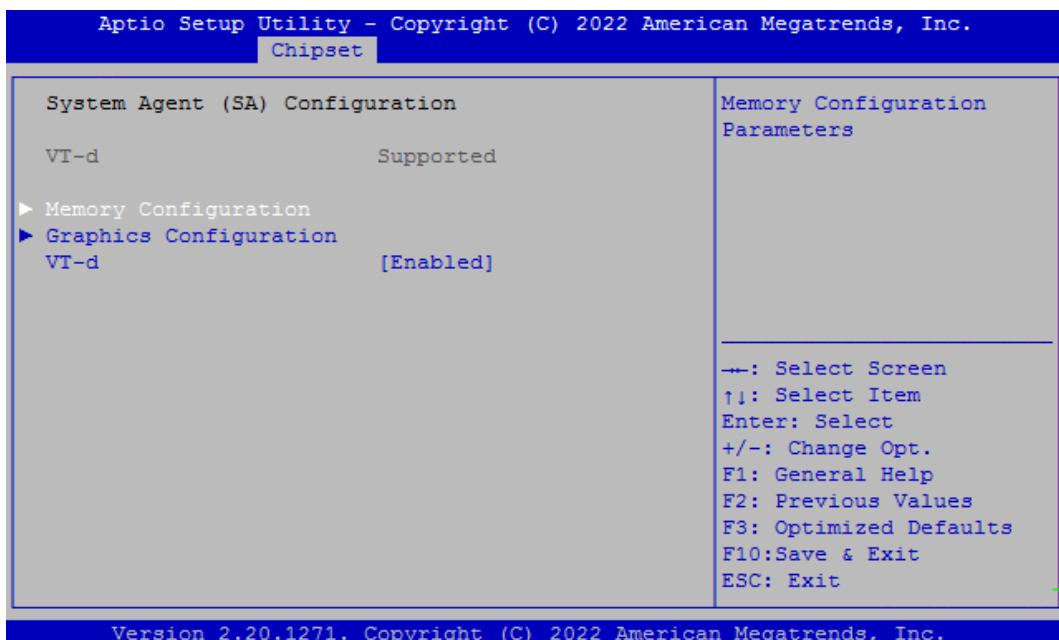


## 4.4 Chipset Setup

This section allows you to configure chipset related settings according to user's preference.



#### 4.4.1 System Agent (SA) Configuration



##### ■ Memory Configuration

This item displays detailed memory configuration in the system.

##### ■ Graphics Configuration

###### Internal Graphics [Auto]

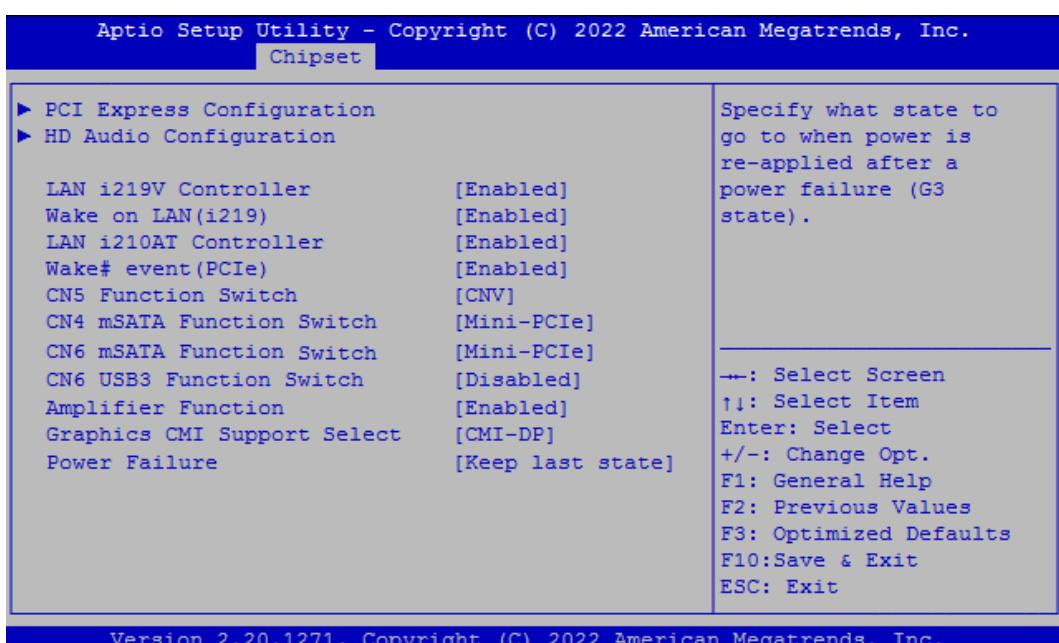
Allows users to enable or disable Internal Graphics.

Configuration options: [Auto] [Disabled] [Enabled]

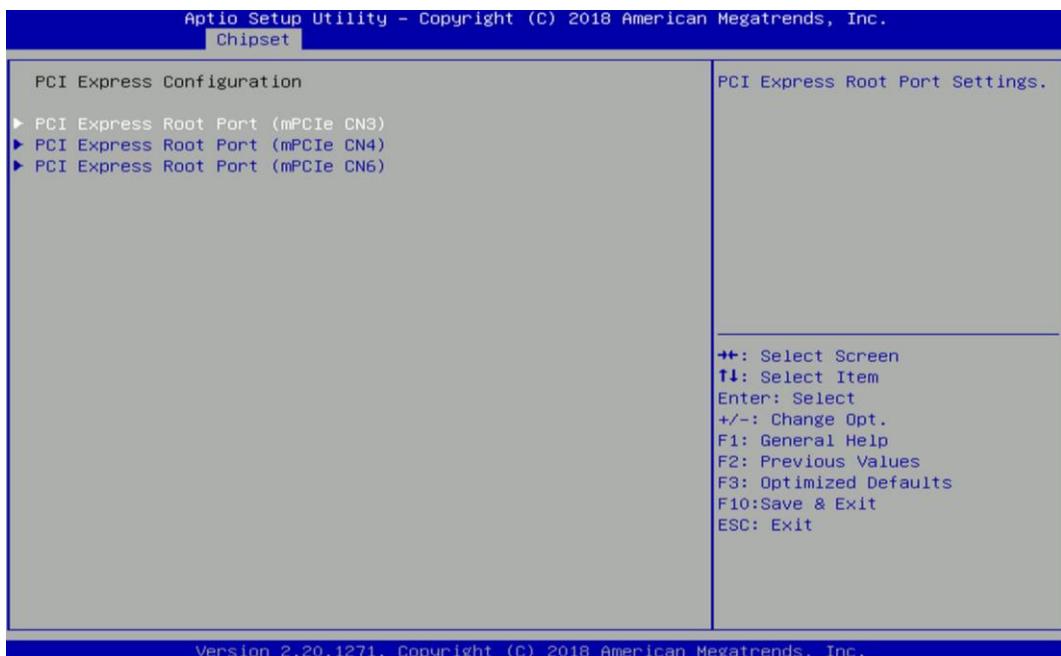
##### ■ VT-d [Enabled]

Enables or disables Intel® Virtualization Technology for Directed I/O (VT-d) capability.

#### 4.4.2 PCH-IO Configuration



## ■ PCI Express Configuration



### PCI Express Root Port (mPCIe CN3)

#### ■ PCI Express Root Port [Enabled]

Enables or disables PCI Express Root Port.

#### ■ PCIe Speed [Auto]

Allows you to select PCI Express interface speed.

Configuration options: [Auto] [Gen1] [Gen2] [Gen3].

### PCI Express Root Port (mPCIe CN4)

#### ■ PCI Express Root Port [Enabled]

Enables or disables PCI Express Root Port.

#### ■ PCIe Speed [Auto]

Allows you to select PCI Express interface speed.

Configuration options: [Auto] [Gen1] [Gen2] [Gen3].

### PCI Express Root Port (mPCIe CN6)

#### ■ PCI Express Root Port [Enabled]

Enables or disables PCI Express Root Port.

#### ■ PCIe Speed [Auto]

Allows you to select PCI Express interface speed.

Configuration options: [Auto] [Gen1] [Gen2] [Gen3].

## ■ HD Audio Configuration

### HD Audio [Enabled]

Enables or disables HD Audio.

## ■ LAN i219V Controller [Enabled]

Enables or disables I219 LAN Controller.

## ■ Wake on LAN (i219) [Enabled]

Enables or disables integrated LAN Wake On LAN function.

**■ LAN i210AT Controller [Enabled]**

Enables or disables I210 LAN Controller.

**■ Wake# event (PCIe) [Enabled]**

Enables or disables Wake# event(PCIe).

**■ CN5 Function Switch [CNV]**

Select [CNV] or [WiFi] for CN5 connector.

**■ CN4 mSATA Function Switch [Mini-PCIe]**

Allows you to change **mPCIe CN4** as [Mini-PCIe] or [mSATA].

**■ CN6 mSATA Function Switch [Mini-PCIe]**

Allows you to change **mPCIe CN6** as [Mini-PCIe] or [mSATA].

**■ CN6 USB3 Function Switch [Disabled]**

Enables or disables CN6 USB3 Controller.

**■ Amplifier Function [Enabled]**

Enables or disables Amplifier Function.

**■ Graphics CMI Support Select [CMI-DP]**

Choose CMI-DP: Support DP & HDMI (2K only)

Choose CMI-HDMI: Only support HDMI (4K)

**■ Power Failure [Keep last state]**

Allows you to specify which power state system will enter when power is resumed after a power failure (G3 state).

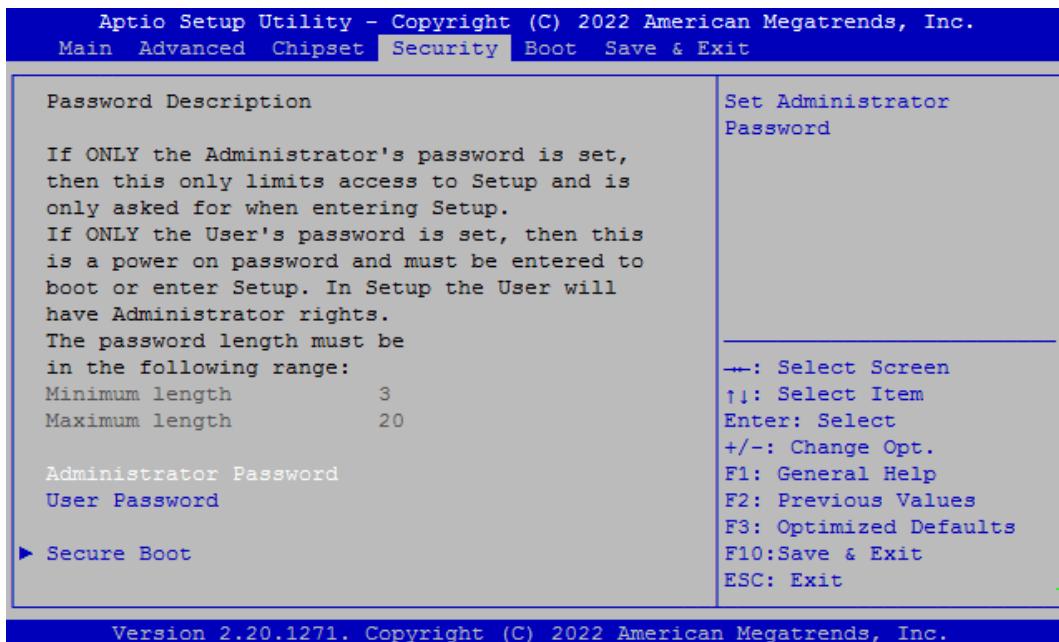
[Always on]: Enters to power on state.

[Always off]: Enters to power off state.

[Keep last state]: Enters to the last power state before a power failure.

## 4.5 Security Setup

This section allows users to configure BIOS security settings.



### 4.5.1 Administrator Password

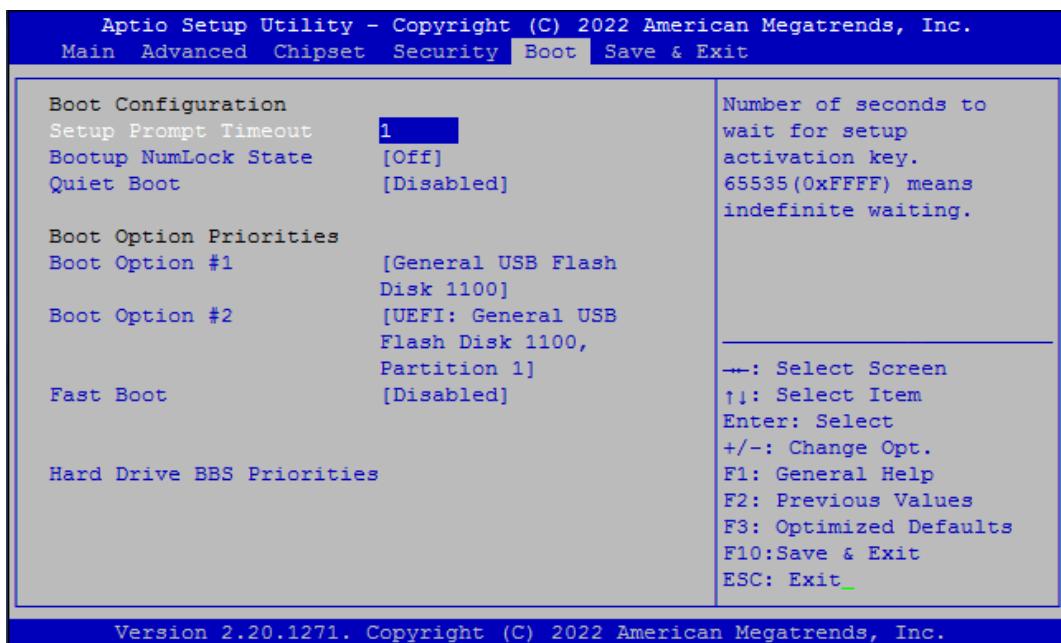
Administrator Password controls access to the BIOS Setup utility.

### 4.5.2 User Password

User Password controls access to the system at boot and to the BIOS Setup utility.

## 4.6 Boot Setup

This section allows you to configure Boot settings.



### 4.6.1 Setup Prompt Timeout

Use this item to set number of seconds (1..65535) to wait for setup activation key.

### 4.6.2 Bootup NumLock State

Allows you to set NumLock key to [On] or [Off] state when system boots up.

### 4.6.3 Quiet Boot

Allows you to enable or disable Quiet Boot function.

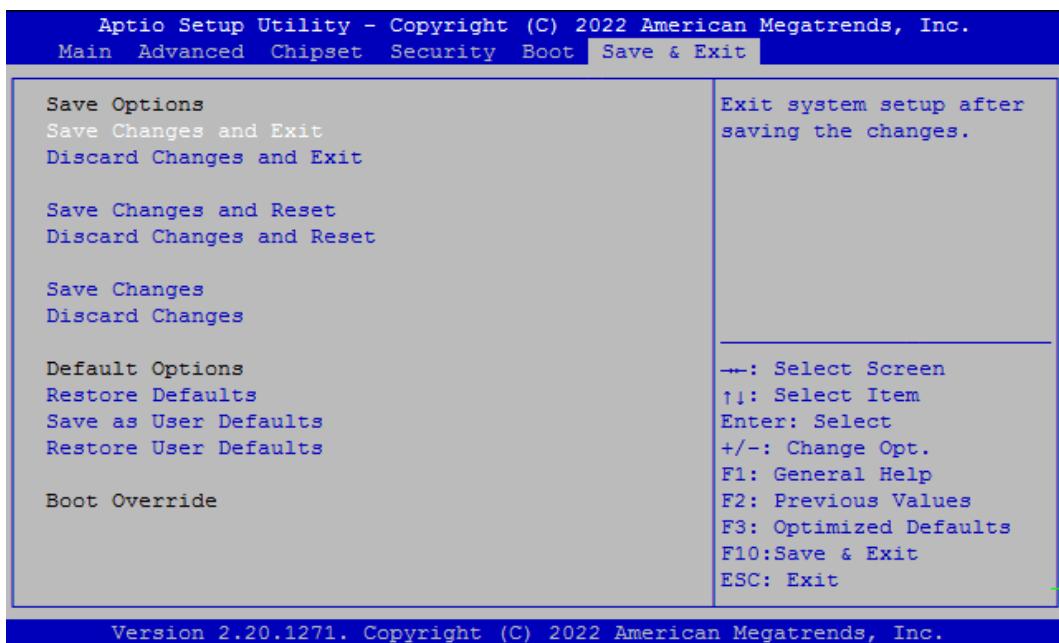
### 4.6.4 Fast Boot

Allows you to enable or disable Fast Boot function. If enabled, system boots with initialization of a minimal set of devices required to launch active boot option.

### 4.6.5 Hard Drive BBS Priority

Allows you to set the order of the legacy devices in this group.

## 4.7 Save & Exit



### 4.7.1 Save Changes and Exit

This item allows you to exit system setup after saving changes.

### 4.7.2 Discard Changes and Exit

This item allows you to exit system setup without saving changes.

### 4.7.3 Save Changes and Reset

This item allows you to reset the system after saving changes.

### 4.7.4 Discard Changes and Reset

This item allows you to reset system setup without saving any changes.

### 4.7.5 Save Changes

This item allows you to save changes done so far to any of the setup options.

### 4.7.6 Discard Changes.

This item allows you to discard changes done so far to any of the setup options.

### 4.7.7 Restore Defaults

This item allows you to restore/ load default values for all the setup options.

### 4.7.8 Save as User Defaults

This item allows you to save the changes done so far as user defaults.

### 4.7.9 Restore User Defaults

This item allows you to restore the user defaults to all the setup options.



# **Chapter 5**

## **Product Application**

## 5.1 Digital I/O (DIO) application

This section describes DIO application of the product. The content and application development are better understood and implemented by well experienced professionals or developers.

### 5.1.1 Digital I/O Programming Guide

#### 5.1.1.1 Pins for Digital I/O 1~8

Item	Standard	Item	Standard
GPIO70 (PIN 103)	DI	GPIO80 (PIN 111)	DO
GPIO71 (PIN 104)		GPIO81 (PIN 112)	
GPIO72 (PIN 105)		GPIO82 (PIN 113)	
GPIO73 (PIN 106)		GPIO83 (PIN 114)	
GPIO74 (PIN 107)		GPIO84 (PIN 115)	
GPIO75 (PIN 108)		GPIO85 (PIN 116)	
GPIO76 (PIN 109)		GPIO86 (PIN 117)	
GPIO77 (PIN 110)		GPIO87 (PIN 118)	

#### 5.1.1.2 Pins for Digital I/O 9~16

Item	Standard	Item	Standard
GPIO30 (PIN 36)	DI	GPIO40 (PIN 44)	DO
GPIO31 (PIN 37)		GPIO41 (PIN 45)	
GPIO32 (PIN 38)		GPIO42 (PIN 46)	
GPIO33 (PIN 39)		GPIO43 (PIN 47)	
GPIO34 (PIN 40)		GPIO44 (PIN 48)	
GPIO35 (PIN 41)		GPIO45 (PIN 49)	
GPIO36 (PIN 42)		GPIO46 (PIN 50)	
GPIO37 (PIN 43)		GPIO47 (PIN 51)	

#### 5.1.1.3 Programming Guide

To program the Super I/O chip F81866A configuration registers, the following configuration procedures must be followed in sequence:

- (1) Enter the Extended Function Mode
- (2) Configure the configuration registers
- (3) Exit the Extended Function Mode

The configuration register is used to control the behavior of the corresponding devices. To configure the register, use the index port to select the index and then write data port to alter

the parameters. The default index port and data port are 0x4E and 0x4F, respectively.

**Pull down the SOUT1 pin to change the default value to 0x2E/ 0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit entry key 0xAA to the index port.**

Following is an example to enable configuration and to disable configuration by using debug.

-o 4e 87

-o 4e 87 (enable configuration)

-o 4e aa (disable configuration)

#### 5.1.1.4 Relative Registers

To program the F81866A configuration registers, see the following configuration procedures.

Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-0	LDN	R/W	LRESET#	00h	00h: Select FDC device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. <b>06h: Select GPIO device configuration registers.</b> 07h: Select WDT device configuration registers. 0Ah: Select PME, ACPI and ERP device configuration registers. 10h: Select UART1 device configuration registers. 11h: Select UART2 device configuration registers. 12h: Select UART3 device configuration registers. 13h: Select UART4 device configuration registers. 14h: Select UART5 device configuration registers. 15h: Select UART6 device configuration registers. Otherwise: Reserved.

#### 8.7.13.1 GPIO7 Output Enable Register — Index 80h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_OE	R/W	LRESET#	0	0: GPIO77 is in input mode. 1: GPIO77 is in output mode.
6	GPIO76_OE	R/W	LRESET#	0	0: GPIO76 is in input mode. 1: GPIO75 is in output mode.
5	GPIO75_OE	R/W	LRESET#	0	0: GPIO75 is in input mode. 1: GPIO75 is in output mode.
4	GPIO74_OE	R/W	LRESET#	0	0: GPIO74 is in input mode. 1: GPIO74 is in output mode.
3	GPIO73_OE	R/W	LRESET#	0	0: GPIO73 is in input mode. 1: GPIO73 is in output mode.
2	GPIO72_OE	R/W	LRESET#	0	0: GPIO72 is in input mode. 1: GPIO72 is in output mode.
1	GPIO71_OE	R/W	LRESET#	0	0: GPIO71 is in input mode. 1: GPIO71 is in output mode.
0	GPIO70_OE	R/W	LRESET#	0	0: GPIO70 is in input mode. 1: GPIO70 is in output mode.

#### 8.7.13.3 GPIO7 Pin Status Register — Index 82h (This byte could be also read by base address + 3)

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_IN	R	-	-	The pin status of GPIO77/STB#.
6	GPIO76_IN	R	-	-	The pin status of GPIO76/AFD#.
5	GPIO75_IN	R	-	-	The pin status of GPIO75/ERR#.
4	GPIO74_IN	R	-	-	The pin status of GPIO74/INIT#.
3	GPIO73_IN	R	-	-	The pin status of GPIO73/SLIN#.
2	GPIO72_IN	R	-	-	The pin status of GPIO72/ACK#.
1	GPIO71_IN	R	-	-	The pin status of GPIO71/BUSY.
0	GPIO70_IN	R	-	-	The pin status of GPIO70/PE/FANCTL3/PWM_DAC3.

#### 8.7.9.1 GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_OE	R/W	LRESET#	0	0: GPIO37 is input. 1: GPIO37 is output.
6	GPIO36_OE	R/W	LRESET#	0	0: GPIO36 is input. 1: GPIO36 is output.
5	GPIO35_OE	R/W	LRESET#	0	0: GPIO35 is input. 1: GPIO35 is output.
4	GPIO34_OE	R/W	LRESET#	0	0: GPIO34 is input. 1: GPIO34 is output.
3	GPIO33_OE	R/W	LRESET#	0	0: GPIO33 is input. 1: GPIO33 is output.
2	GPIO32_OE	R/W	LRESET#	0	0: GPIO32 is input. 1: GPIO32 is output.
1	GPIO31_OE	R/W	LRESET#	0	0: GPIO31 is input. 1: GPIO31 is output.
0	GPIO30_OE	R/W	LRESET#	0	0: GPIO30 is input. 1: GPIO30 is output.

#### 8.7.9.3 GPIO3 Pin Status Register — Index C2h (This byte could be also read by base address + 9 if **GPIO\_DEC\_RANGE** is set to "1")

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_IN	R	-	-	The pin status of SIN3/GPIO37.
6	GPIO36_IN	R	-	-	The pin status of SOUT3/GPIO36.
5	GPIO35_IN	R	-	-	The pin status of DSR3#/GPIO35.
4	GPIO34_IN	R	-	-	The pin status of RTS3#/GPIO34.
3	GPIO33_IN	R	-	-	The pin status of DTR3#/GPIO33.
2	GPIO32_IN	R	-	-	The pin status of CTS3#/GPIO32.
1	GPIO31_IN	R	-	-	The pin status of RI3#/GPIO31.
0	GPIO30_IN	R	-	-	The pin status of DCD3#/GPIO30.

#### 8.7.14.1GPIO8 Output Enable Register — Index 88h

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_OE	R/W	LRESET#	1	0: GPIO87 is in input mode. 1: GPIO87 is in output mode.
6	GPIO86_OE	R/W	LRESET#	1	0: GPIO86 is in input mode. 1: GPIO86 is in output mode.
5	GPIO85_OE	R/W	LRESET#	1	0: GPIO85 is in input mode. 1: GPIO85 is in output mode.
4	GPIO84_OE	R/W	LRESET#	1	0: GPIO84 is in input mode. 1: GPIO84 is in output mode.
3	GPIO83_OE	R/W	LRESET#	1	0: GPIO83 is in input mode. 1: GPIO83 is in output mode.
2	GPIO82_OE	R/W	LRESET#	1	0: GPIO82 is in input mode. 1: GPIO82 is in output mode.
1	GPIO81_OE	R/W	LRESET#	1	0: GPIO81 is in input mode. 1: GPIO81 is in output mode.
0	GPIO80_OE	R/W	LRESET#	1	0: GPIO80 is in input mode. 1: GPIO80 is in output mode.

#### 8.7.14.2GPIO8 Output Data Register — Index 89h (This byte could be also written by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_VAL	R/W	LRESET#	1	0: GPIO87 outputs 0 when in output mode. 1: GPIO87 outputs 1 when in output mode.
6	GPIO86_VAL	R/W	LRESET#	1	0: GPIO86 outputs 0 when in output mode. 1: GPIO86 outputs 1 when in output mode.
5	GPIO85_VAL	R/W	LRESET#	1	0: GPIO85 outputs 0 when in output mode. 1: GPIO85 outputs 1 when in output mode.
4	GPIO84_VAL	R/W	LRESET#	1	0: GPIO84 outputs 0 when in output mode. 1: GPIO84 outputs 1 when in output mode.
3	GPIO83_VAL	R/W	LRESET#	1	0: GPIO83 outputs 0 when in output mode. 1: GPIO83 outputs 1 when in output mode.
2	GPIO82_VAL	R/W	LRESET#	1	0: GPIO82 outputs 0 when in output mode. 1: GPIO82 outputs 1 when in output mode.
1	GPIO81_VAL	R/W	LRESET#	1	0: GPIO81 outputs 0 when in output mode. 1: GPIO81 outputs 1 when in output mode.
0	GPIO80_VAL	R/W	LRESET#	1	0: GPIO80 outputs 0 when in output mode. 1: GPIO80 outputs 1 when in output mode.

#### 8.7.10.1GPIO4 Output Enable Register — Index B0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_OE	R/W	LRESET#	1	0: GPIO47 is input. 1: GPIO47 is output.
6	GPIO46_OE	R/W	LRESET#	1	0: GPIO46 is input. 1: GPIO46 is output.
5	GPIO45_OE	R/W	LRESET#	1	0: GPIO45 is input. 1: GPIO45 is output.
4	GPIO44_OE	R/W	LRESET#	1	0: GPIO44 is input. 1: GPIO44 is output.
3	GPIO43_OE	R/W	LRESET#	1	0: GPIO43 is input. 1: GPIO43 is output.
2	GPIO42_OE	R/W	LRESET#	1	0: GPIO42 is input. 1: GPIO42 is output.
1	GPIO41_OE	R/W	LRESET#	1	0: GPIO41 is input. 1: GPIO41 is output.
0	GPIO40_OE	R/W	LRESET#	1	0: GPIO40 is input. 1: GPIO40 is output.

**8.7.10.2GPIO4 Output Data Register — Index B1h (This byte could be also written by base address + 10 if GPIO\_DEC\_RANGE is set to “1”)**

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_DATA	R/W	LRESET#	1	0: GPIO47 outputs 0 when in output mode. 1: GPIO47 outputs 1 when in output mode.
6	GPIO46_DATA	R/W	LRESET#	1	0: GPIO46 outputs 0 when in output mode. 1: GPIO46 outputs 1 when in output mode.
5	GPIO45_DATA	R/W	LRESET#	1	0: GPIO45 outputs 0 when in output mode. 1: GPIO45 outputs 1 when in output mode.
4	GPIO44_DATA	R/W	LRESET#	1	0: GPIO44 outputs 0 when in output mode. 1: GPIO44 outputs 1 when in output mode.
3	GPIO43_DATA	R/W	LRESET#	1	0: GPIO43 outputs 0 when in output mode. 1: GPIO43 outputs 1 when in output mode.
2	GPIO42_DATA	R/W	LRESET#	1	0: GPIO42 outputs 0 when in output mode. 1: GPIO42 outputs 1 when in output mode.
1	GPIO41_DATA	R/W	LRESET#	1	0: GPIO41 outputs 0 when in output mode. 1: GPIO41 outputs 1 when in output mode.
0	GPIO40_DATA	R/W	LRESET#	1	0: GPIO40 outputs 0 when in output mode. 1: GPIO40 outputs 1 when in output mode.

**8.7.3Base Address High Register — Index 60h**

Bit	Name	R/W	Reset	Default	Description
7-0	GP_BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of GPIO I/O port address.

**8.7.3.4Base Address Low Register — Index 61h**

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	00h	<p>The LSB of KBC data port address. When GPIO_DEC_RANGE is “0”, only 8 bytes are decoded:</p> <p>Base + 0: index port.      Base + 1: data port.      Base + 2: GPIO8 data register.      Base + 3: GPIO7 data register.      Base + 4: GPIO6 data register.      Base + 5: GPIO5 data register.      Base + 6: GPIO0 data register.      Base + 7: GPIO1 data register.</p> <p>If GPIO_DEC_RANGE is set to “1”, more 8 bytes are decoded:</p> <p>Base + 8: GPIO2 data register.      Base + 9: GPIO3 data register.      Base + 10: GPIO4 data register.</p> <p>Otherwise: Reserved.</p> <p>There are three ways to access the GPIO registers.</p> <ol style="list-style-type: none"> <li>1. Use configuration register port 0x4E/0x4F (or 0x2E/0x2F), the LDN for GPIO is 0x06.</li> <li>2. Use GPIO index/data port. Write index to index port first and then read/write the register.</li> <li>3. Use digital I/O port. The way only access GPIO data register. Write data to this port will control the data output register. And read this port will read the pin status register.</li> </ol>

### 5.1.1.5 Sample Code in C Language

#### 5.1.1.5.1 Control of GP70 to GP77 (DI1 ~ DI8)

```
#define AddrPort 0x4E  
#define DataPort 0x4F
```

<Enter the Extended Function Mode>

```
WriteByte(AddrPort, 0x87)  
WriteByte(AddrPort, 0x87) // Must write twice to enter Extended mode
```

<Select Logic Device>

```
WriteByte(AddrPort, 0x07)  
WriteByte(DataPort, 0x06) // Select logic device 06h
```

<Output/Input Mode Selection>

```
WriteByte(AddrPort, 0x80) // Set GP70 to GP77 input Mode  
WriteByte(DataPort, 0x0X) // Select configuration register 80h  
// Set (bit 0~7) = 0 to select GP 70~77 as Input mode.
```

<Input Value>

```
WriteByte(AddrPort, 0x82) // Select configuration register 82h  
ReadByte(DataPort, Value) // Read bit 0~7 (0xFx)= GP70 ~77 as High.
```

<Leave the Extended Function Mode>

```
WriteByte(AddrPort, 0xAA)
```

#### 5.1.1.5.2 Control of GP80 to GP87 (DO1 ~ DO8)

```
#define AddrPort 0x4E  
#define DataPort 0x4F
```

<Enter the Extended Function Mode>

```
WriteByte(AddrPort, 0x87)  
WriteByte(AddrPort, 0x87) // Must write twice to enter Extended mode
```

<Select Logic Device>

```
WriteByte(AddrPort, 0x07)  
WriteByte(DataPort, 0x06) // Select logic device 06h
```

<Output/Input Mode Selection>

```
WriteByte(AddrPort, 0x88) // Set GP80 to GP87 output Mode  
WriteByte(DataPort, 0XF) // Select configuration register 88h  
// Set (bit 0~7) = 1 to select GP 80 ~87 as Output mode.
```

<Output Value>

```
WriteByte(AddrPort, 0x89)          // Select configuration register 89h  
WriteByte(DataPort, Value)         // Set bit 0~7=(0/1) to output GP 80~87 as Low or High  
  
<Leave the Extended Function Mode>  
WriteByte(AddrPort, 0xAA)
```

#### 5.1.1.5.3 Control of GP70 to GP77 & GP30 to GP37 (DI1 ~ DI16)

```
#define AddrPort 0x4E  
#define DataPort 0x4F
```

<Enter the Extended Function Mode>

```
WriteByte(AddrPort, 0x87)  
WriteByte(AddrPort, 0x87)          // Must write twice to entering Extended mode
```

<Select Logic Device>

```
WriteByte(AddrPort, 0x07)  
WriteByte(DataPort, 0x06)          // Select logic device 06h
```

<Input Mode Selection>

```
WriteByte(AddrPort, 0x80)          // Set GP70 to GP77 input Mode  
WriteByte(DataPort, 0x0X)          // Select configuration register 80h  
                                // Set (bit 0~7) = 0 to select GP 70~77 as Input mode
```

<Input Mode Selection>

```
WriteByte(AddrPort, 0xC0)          // Set GP30 to GP37 input Mode  
WriteByte(DataPort, 0x0X)          // Select configuration register C0h  
                                // Set (bit 0~7) = 0 to select GP 30~37 as Input mode
```

<input Value>

```
WriteByte(AddrPort, 0x82)          // Select configuration register 82h  
ReadByte(DataPort, Value)         // Read bit 0~7(0xFx)= GP70~77 as High
```

<input Value>

```
WriteByte(AddrPort, 0xC2)          // Select configuration register C2h  
ReadByte(DataPort, Value)         // Read bit 0~7(0xFx)= GP30~37 as High
```

<Leave the Extended Function Mode>

```
WriteByte(AddrPort, 0xAA)
```

#### 5.1.1.5.4 Control of GP80 to GP87 & GP40 to GP47 (DO1 ~ DO16)

```
#define AddrPort 0x4E  
#define DataPort 0x4F
```

<Enter the Extended Function Mode>

```
WriteByte(AddrPort, 0x87)  
WriteByte(AddrPort, 0x87)           // Must write twice to entering Extended mode
```

<Select Logic Device>

```
WriteByte(AddrPort, 0x07)  
WriteByte(DataPort, 0x06)           // Select logic device 06h
```

<Output Mode Selection>

```
WriteByte(AddrPort, 0x88)           // Set GP80 to GP87 output Mode  
WriteByte(DataPort, (0XF))         // Select configuration register 88h  
                                  // Set (bit 0~7) = 1 to select GP 80~87 as Output mode
```

<Output Mode Selection>

```
WriteByte(AddrPort, 0xB0)           // Set GP40 to GP47 output Mode  
WriteByte(DataPort, (0XF))         // Select configuration register B0h  
                                  // Set (bit 0~7) = 1 to select GP 40~47 as Output mode
```

<Output Value>

```
WriteByte(AddrPort, 0x89)           // Select configuration register 89h  
WriteByte(DataPort, Value)          // Set bit 0~7=(0/1) to output GP 80~87 as Low or High
```

<Output Value>

```
WriteByte(AddrPort, 0xB1)           // Select configuration register B1h  
WriteByte(DataPort, Value)          // Set bit 0~7=(0/1) to output GP 40~47 as Low or High
```

<Leave the Extended Function Mode>

```
WriteByte(AddrPort, 0xAA)
```

#### 5.1.1.6 Change base address

<Enter the Extended Function Mode>

```
WriteByte(AddrPort, 0x87)  
WriteByte(AddrPort, 0x87)           // Must write twice to enter Extended mode
```

<Select Logic Device>

```
WriteByte(AddrPort, 0x07)  
WriteByte(DataPort, 0x06)           // Select logic device 06h
```

```
WriteByte(AddrPort, 0x60)          // Select configuration register 60h (High Byte address)
WriteByte(DataPort, (0x0A))

WriteByte(AddrPort, 0x61)          // Select configuration register 61h (Low Byte address)
WriteByte(DataPort, (0x00))

<Leave the Extended Function Mode>
WriteByte(AddrPort, 0xAA)
```

Cincoze default GPIO Port base address is 0xA00h

### 5.1.1.7 DATA Bit Table (DIO)

<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Value</td></tr> <tr><td colspan="8">1</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	0	1	Value	1								/h	= DI1 (Base address +3) (0xA03)	<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Value</td></tr> <tr><td colspan="8">1</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	0	1	Value	1								/h	= DO1 (Base address +2) (0xA02)	
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	0	0	0	1	Value																																																		
1								/h																																																		
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	0	0	0	1	Value																																																		
1								/h																																																		
<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">2</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	1	0	Value	2								/h	= DI2 (Base address +3) (0xA03)	<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">2</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	0	1	0	Value	2								/h	= DO2 Base address +2) (0xA02)
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	0	0	1	0	Value																																																		
2								/h																																																		
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	0	0	0	1	0	Value																																																	
2								/h																																																		
<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">4</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	1	0	0	Value	4								/h	= DI3 (Base address +3) (0xA03)	<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">4</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	1	0	0	Value	4								/h	= DO3 Base address +2) (0xA02)
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	0	1	0	0	Value																																																		
4								/h																																																		
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	0	0	1	0	0	Value																																																	
4								/h																																																		
<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">8</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	1	0	0	0	Value	8								/h	= DI4 (Base address +3) (0xA03)	<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">8</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	1	0	0	0	Value	8								/h	= DO4 Base address +2) (0xA02)	
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	1	0	0	0	Value																																																		
8								/h																																																		
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	1	0	0	0	Value																																																		
8								/h																																																		
<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">10</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	1	0	0	0	0	Value	10								/h	= DI5 (Base address +3) (0xA03)	<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">10</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	1	0	0	0	0	Value	10								/h	= DO5 Base address +2) (0xA02)	
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	1	0	0	0	0	Value																																																		
10								/h																																																		
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	1	0	0	0	0	Value																																																		
10								/h																																																		
<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">20</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	1	0	0	0	0	0	Value	20								/h	= DI6 (Base address +3) (0xA03)	<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">20</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	1	0	0	0	0	0	Value	20								/h	= DO6 Base address +2) (0xA02)	
7	6	5	4	3	2	1	0	bit																																																		
0	0	1	0	0	0	0	0	Value																																																		
20								/h																																																		
7	6	5	4	3	2	1	0	bit																																																		
0	0	1	0	0	0	0	0	Value																																																		
20								/h																																																		
<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">40</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	1	0	0	0	0	0	0	Value	40								/h	= DI7 (Base address +3) (0xA03)	<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">40</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	1	0	0	0	0	0	0	Value	40								/h	= DO7 Base address +2) (0xA02)	
7	6	5	4	3	2	1	0	bit																																																		
0	1	0	0	0	0	0	0	Value																																																		
40								/h																																																		
7	6	5	4	3	2	1	0	bit																																																		
0	1	0	0	0	0	0	0	Value																																																		
40								/h																																																		
<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">80</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	1	0	0	0	0	0	0	0	Value	80								/h	= DI8 (Base address +3) (0xA03)	<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr> <tr><td colspan="8">80</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	1	0	0	0	0	0	0	0	Value	80								/h	= DO8 Base address +2) (0xA02)	
7	6	5	4	3	2	1	0	bit																																																		
1	0	0	0	0	0	0	0	Value																																																		
80								/h																																																		
7	6	5	4	3	2	1	0	bit																																																		
1	0	0	0	0	0	0	0	Value																																																		
80								/h																																																		
<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Value</td></tr> <tr><td colspan="8">1</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	0	1	Value	1								/h	= DI9 (Base address +9) (0xA09)	<table border="1"> <tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Value</td></tr> <tr><td colspan="8">1</td><td>/h</td></tr> </table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	0	0	1	Value	1								/h	= DO9 (Base address +10) (0xA10)
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	0	0	0	1	Value																																																		
1								/h																																																		
7	6	5	4	3	2	1	0	bit																																																		
0	0	0	0	0	0	0	0	1	Value																																																	
1								/h																																																		

<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Value</td></tr><tr><td colspan="8">2</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	1	0	Value	2								/h	= DI10 (Base address +9) (0xA09)	<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td colspan="8">2</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	0	1	0	2								/h	= DO10 Base address +10) (0xA10)
7	6	5	4	3	2	1	0	bit																																																	
0	0	0	0	0	0	1	0	Value																																																	
2								/h																																																	
7	6	5	4	3	2	1	0	bit																																																	
0	0	0	0	0	0	0	1	0																																																	
2								/h																																																	
<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">4</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	1	0	0	Value	4								/h	= DI11 (Base address +9) (0xA09)	<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td colspan="8">4</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	0	0	1	0	0	4								/h	= DO11 Base address +10) (0xA10)
7	6	5	4	3	2	1	0	bit																																																	
0	0	0	0	0	1	0	0	Value																																																	
4								/h																																																	
7	6	5	4	3	2	1	0	bit																																																	
0	0	0	0	0	0	1	0	0																																																	
4								/h																																																	
<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">8</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	1	0	0	0	Value	8								/h	= DI12 (Base address +9) (0xA09)	<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">8</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	0	0	1	0	0	0	Value	8								/h	= DO12 Base address +10) (0xA10)
7	6	5	4	3	2	1	0	bit																																																	
0	0	0	0	1	0	0	0	Value																																																	
8								/h																																																	
7	6	5	4	3	2	1	0	bit																																																	
0	0	0	0	1	0	0	0	Value																																																	
8								/h																																																	
<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">10</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	0	1	0	0	0	0	Value	10								/h	= DI13 (Base address +9) (0xA09)	<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">10</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	0	1	0	0	0	0	Value	10								/h	= DO13 Base address +10) (0xA10)
7	6	5	4	3	2	1	0	bit																																																	
0	0	0	1	0	0	0	0	Value																																																	
10								/h																																																	
7	6	5	4	3	2	1	0	bit																																																	
0	0	0	1	0	0	0	0	Value																																																	
10								/h																																																	
<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">20</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	1	0	0	0	0	0	Value	20								/h	= DI14 (Base address +9) (0xA09)	<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">20</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	0	1	0	0	0	0	0	Value	20								/h	= DO14 Base address +10) (0xA10)
7	6	5	4	3	2	1	0	bit																																																	
0	0	1	0	0	0	0	0	Value																																																	
20								/h																																																	
7	6	5	4	3	2	1	0	bit																																																	
0	0	1	0	0	0	0	0	Value																																																	
20								/h																																																	
<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">40</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	1	0	0	0	0	0	0	Value	40								/h	= DI15 (Base address +9) (0xA09)	<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">40</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	0	1	0	0	0	0	0	0	Value	40								/h	= DO15 Base address +10) (0xA10)
7	6	5	4	3	2	1	0	bit																																																	
0	1	0	0	0	0	0	0	Value																																																	
40								/h																																																	
7	6	5	4	3	2	1	0	bit																																																	
0	1	0	0	0	0	0	0	Value																																																	
40								/h																																																	
<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">80</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	1	0	0	0	0	0	0	0	Value	80								/h	= DI16 (Base address +9) (0xA09)	<table border="1"><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>bit</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Value</td></tr><tr><td colspan="8">80</td><td>/h</td></tr></table>	7	6	5	4	3	2	1	0	bit	1	0	0	0	0	0	0	0	Value	80								/h	= DO16 Base address +10) (0xA10)
7	6	5	4	3	2	1	0	bit																																																	
1	0	0	0	0	0	0	0	Value																																																	
80								/h																																																	
7	6	5	4	3	2	1	0	bit																																																	
1	0	0	0	0	0	0	0	Value																																																	
80								/h																																																	

### 5.1.1.8 DIO I/O Port Address (Default Address 0xA00)

Pin Definition	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1
Data Bits	7	6	5	4	3	2	1	0
DIO	Digital Input							
I/O Port Address	0xA03							

Pin Definition	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1
Data Bits	7	6	5	4	3	2	1	0
DIO	Digital Output							
I/O Port Address	0xA02							

Pin Definition	DI16	DI15	DI14	DI13	DI12	DI11	DI10	DI9
Data Bits	7	6	5	4	3	2	1	0
DIO	Digital Input							
I/O Port Address	0xA09							

Pin Definition	DO16	DO15	DO14	DO13	DO12	DO11	DO10	DO9
Data Bits	7	6	5	4	3	2	1	0
DIO	Digital Output							
I/O Port Address	0xA010							

## 5.2 DIO Hardware Specification

- XCOM+/ 2XCOM+: Isolated power in V+
- XCOM-/ 2XCOM-: Isolated power in V-
- Isolated power in DC voltage: 9-30V
- 8x / 16x Digital Input (Source Type)
- Input Signal Voltage Level
  - Signal Logic 0: XCOM+ = 9V, Signal Low - V- < 1V  
XCOM+ > 9V, V+ - Signal Low > 8V
  - Signal Logic 1: > XCOM+ - 3V
- Input Driving Sink Current:
  - Minimal: 1 mA
  - Normal: 5 mA
- 8x / 16x Digital Output (Open Drain)
  - DO Signal have to pull up resistor to XCOM+ for external device, the resistance will affect the pull up current
  - Signal High Level: Pull up resistor to XCOM+
  - Signal Low Level: = XCOM-
  - Sink Current: 1A (Max)

## 5.2.1 DIO Connector Definition

BTB\_FH1

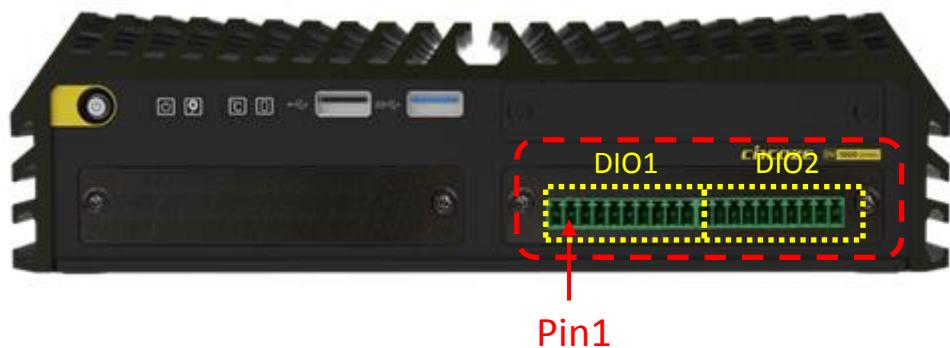


### DIO1/DIO2: Digital Input / Output Connector

Connector Type: Terminal Block 1X20 20-pin, 3.5mm pitch

Pin	Definition	Pin	Definition
1	XCOM+ (DC INPUT)	11	XCOM+ (DC INPUT)
2	DI1	12	DO1
3	DI2	13	DO2
4	DI3	14	DO3
5	DI4	15	DO4
6	DI5	16	DO5
7	DI6	17	DO6
8	DI7	18	DO7
9	DI8	19	DO8
10	XCOM- (GND)	20	XCOM- (GND)

## **BTB\_FH2**

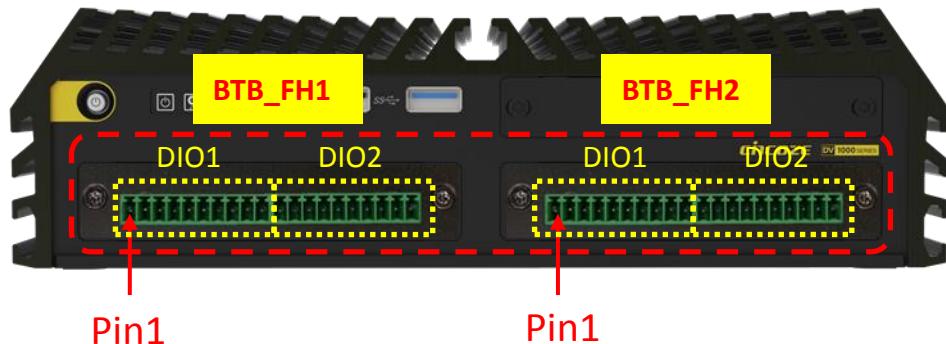


### **DIO1/DIO2: Digital Input / Output Connector**

Connector Type: Terminal Block 1X20 20-pin, 3.5mm pitch

<b>Pin</b>	<b>Definition</b>	<b>Pin</b>	<b>Definition</b>
1	XCOM+ (DC INPUT)	11	XCOM+ (DC INPUT)
2	DI1	12	DO1
3	DI2	13	DO2
4	DI3	14	DO3
5	DI4	15	DO4
6	DI5	16	DO5
7	DI6	17	DO6
8	DI7	18	DO7
9	DI8	19	DO8
10	XCOM- (GND)	20	XCOM- (GND)

## **BTB\_FH1 & BTB\_FH2**

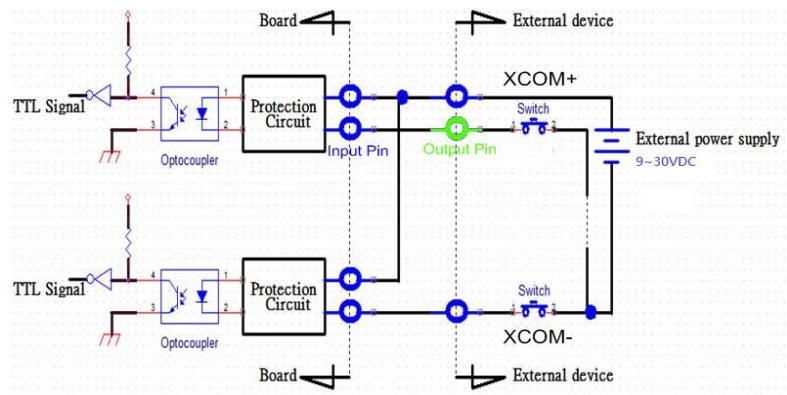


### **DIO1/DIO2: Digital Input / Output Connector**

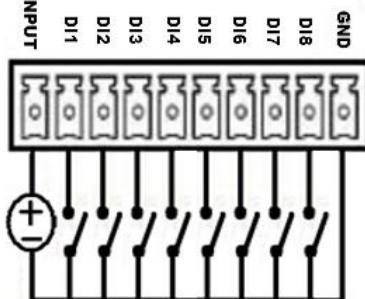
Connector Type: 2 Terminal Block 1X10, 2x20-pin, 3.5mm pitch

BTB_FH1				BTB_FH2			
Pin	DIO1 Definition	Pin	DIO2 Definition	Pin	DIO1 Definition	Pin	DIO2 Definition
1	XCOM+ (DC INPUT)	11	XCOM+ (DC INPUT)	1	XCOM+ (DC INPUT)	11	XCOM+ (DC INPUT)
2	DI9	12	DO9	2	DI1	12	DO1
3	DI10	13	DO10	3	DI2	13	DO2
4	DI11	14	DO11	4	DI3	14	DO3
5	DI12	15	DO12	5	DI4	15	DO4
6	DI13	16	DO13	6	DI5	16	DO5
7	DI14	17	DO14	7	DI6	17	DO6
8	DI15	18	DO15	8	DI7	18	DO7
9	DI16	19	DO16	9	DI8	19	DO8
10	XCOM- (GND)	20	XCOM- (GND)	10	XCOM- (GND)	20	XCOM- (GND)

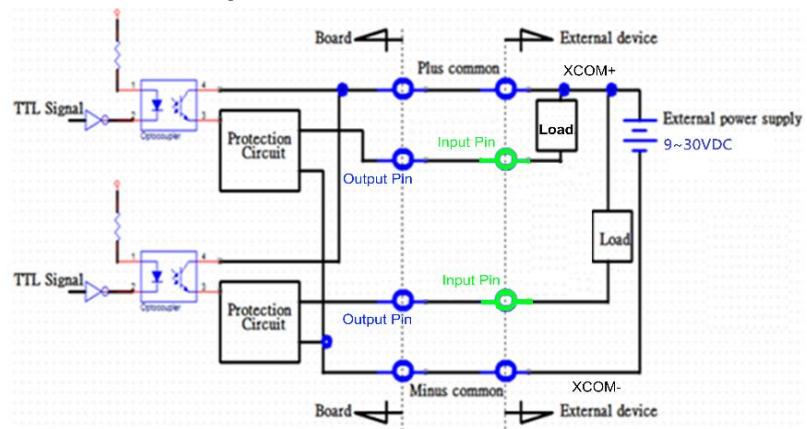
## Reference Input Circuit



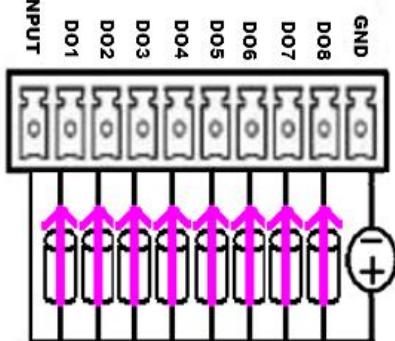
Digital Input Wiring



## Reference Output Circuit



Digital Output Wiring



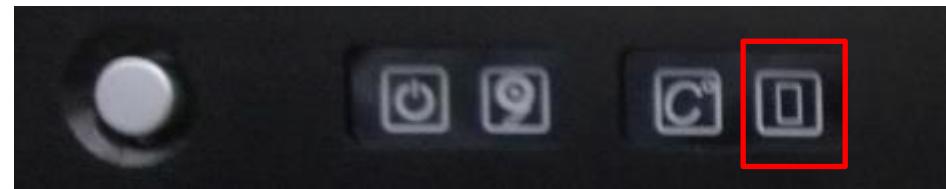
## 5.3 GPIO LED application

This section describes GPIO LED application of the product. The content and application development are better understood and implemented by well experienced professionals or developers.

### 5.3.1 GPIO LED Programming Guide

#### 5.3.1.1 Pins for GPIO LED

GPIO LED



Item	GPIO LED
GPIO 00	LED ON/OFF

#### 5.3.1.2 Programming Guide

To program the Super I/O chip F81866A configuration registers, the following configuration procedures must be followed in sequence:

- (1) Enter the Extended Function Mode
- (2) Configure the configuration registers
- (3) Exit the Extended Function Mode

The configuration register is used to control the behavior of the corresponding devices. To configure the register, use the index port to select the index and then write data port to alter the parameters. The default index port and data port are 0x4E and 0x4F, respectively.

**Pull down the SOUT1 pin to change the default value to 0x2E/ 0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit entry key 0xAA to the index port.**

Following is examples to enable configuration and to disable configuration by using debug.

Example to enable configuration:

```
-o 4e 87  
-o 4e 87
```

Example to disable configuration:

```
-o 4e aa
```

### 5.3.1.3 Relative Registers

To program the F81866A configuration registers, see the following configuration procedures.

Logic Device Number Register (LDN) — Index 07h					
Bit	Name	R/W	Reset	Default	Description
7-0	LDN	R/W	LRESET#	00h	00h: Select FDC device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. <b>06h: Select GPIO device configuration registers.</b> 07h: Select WDT device configuration registers. 0Ah: Select PME, ACPI and ERP device configuration registers. 10h: Select UART1 device configuration registers. 11h: Select UART2 device configuration registers. 12h: Select UART3 device configuration registers. 13h: Select UART4 device configuration registers. 14h: Select UART5 device configuration registers. 15h: Select UART6 device configuration registers. Otherwise: Reserved.

Following is an example to Select GPIO device by LDN(index 07h) using debug.

```
-o 4e 07
-o 4f 06
```

Relative Registers for GPIO LED ( GPIO10)

GPIO0 Output Enable Register — Index F0h					
Bit	Name	R/W	Reset	Default	Description
7	GPIO07_OE	R/W	5VSB	0	0: GPIO07 is input. 1: GPIO07 is output.
6	GPIO06_OE	R/W	5VSB	0	0: GPIO06 is input. 1: GPIO06 is output.
5	GPIO05_OE	R/W	5VSB	0	0: GPIO05 is input. 1: GPIO05 is output.
4	GPIO04_OE	R/W	5VSB	0	0: GPIO04 is input. 1: GPIO04 is output.
3	GPIO03_OE	R/W	5VSB	0	0: GPIO03 is input. 1: GPIO03 is output.
2	GPIO02_OE	R/W	5VSB	0	0: GPIO02 is input. 1: GPIO02 is output.
1	GPIO01_OE	R/W	5VSB	0	0: GPIO01 is input. 1: GPIO01 is output.
0	GPIO00_OE	R/W	5VSB	0	0: GPIO00 is input. <b>1: GPIO00 is output.</b>

Following example to set output enable for GPIO00 ( LED ON/OFF) by using debug.

First step, read the original value from output enable register (index F0)

```
-o 4e f0
-l 4f
```

00 (Note: This is for example, we pretend to get original value is 00 )

Because we need to set bit0 to 1 for GPIO00 output , thus made the new value to 01 .

Second step, write the new value 01 to set bit0 with output mode

-o 4e f0  
-o 4f 01

**GPIO0 Output Data Register — Index F1h (This byte could be also written by base address + 6)**

Bit	Name	R/W	Reset	Default	Description
0	GPIO00_VAL	R/W	5VSB	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode.

Following example to set output data for GPIO00 ( LED ON/OFF) by using debug.

First step, read the original value from output enable register (index F1)

-o 4e f1  
-l 4f

00 (Note: This is for example, we pretend to get original value is 00 )

Because we need to set bit0 to 1 for GPIO00 output data , thus made the new value to 01 .

Second step: write the new value 01 to set bit0 for control output

-o 4e f1  
-o 4f 01 ( Note, the bit0 (GPIO00) can be set 0 or 1 )

#### 5.3.1.4 Sample Code in C Language

Control of GPIO00 ( GPIO LED ON/OFF)

```
#define AddrPort 0x4E
#define DataPort 0x4F

<Enter the Extended Function Mode>
WriteByte(AddrPort, 0x87)
WriteByte(AddrPort, 0x87)      // Must write twice to enter Extended mode

<Select Logic Device>
WriteByte(AddrPort, 0x07)
WriteByte(DataPort, 0x06)      // Select logic device 06h

<Output/Input Mode Selection> // Set GPIO10 to output Mode
WriteByte(AddrPort, 0xF0)      // Select configuration register E0h
Value=ReadByte(DataPort)      //Read Original Value from register E0h
WriteByte(AddrPort, 0xF0)      // Select configuration register E0h
WriteByte(DataPort, Value | 0x01) // Set (bit 0) = 1 to select GPIO10 as output mode

<Output Value>

WriteByte(AddrPort, 0xF1)      // Select configuration register E1h
Value=ReadByte(DataPort)      //Read Original Value from register E1h

WriteByte(AddrPort, 0xF1)      // Select configuration register E1h
WriteByte(DataPort, Value & 0xFE ) // Set (bit 0) =0 to output GPIO10 as Low

WriteByte(AddrPort, 0xF1)      // Select configuration register E1h
WriteByte(DataPort, Value | 0x01 ) // Set (bit 0) =1 to output GPIO10 as High

<Leave the Extended Function Mode>
WriteByte(AddrPort, 0xAA)
```

### 5.3.1.5 Change base address

Cincoze default GPIO Port base address is 0xA00

**Base Address High Register — Index 60h**

Bit	Name	R/W	Reset	Default	Description
7-0	GP_BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of GPIO I/O port address.

**Base Address Low Register — Index 61h**

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	00h	<p>The LSB of KBC data port address. When GPIO_DEC_RANGE is "0", only 8 bytes are decoded:</p> <p>Base + 0: index port.      Base + 1: data port.      Base + 2: GPIO8 data register.      Base + 3: GPIO7 data register.      Base + 4: GPIO6 data register.      Base + 5: GPIO5 data register.  <b>Base + 6: GPIO0 data register.</b> <span style="border: 2px solid red; padding: 2px;">(This row is highlighted)</span>      Base + 7: GPIO1 data register.</p> <p>If GPIO_DEC_RANGE is set to "1", more 8 bytes are decoded:</p> <p>Base + 8: GPIO2 data register.      Base + 9: GPIO3 data register.      Base + 10: GPIO4 data register.</p> <p>Otherwise: Reserved.</p> <p>There are three ways to access the GPIO registers.</p> <ol style="list-style-type: none"> <li>1. Use configuration register port 0x4E/0x4F (or 0x2E/0x2F), the LDN for GPIO is 0x06.</li> <li>2. Use GPIO index/data port. Write index to index port first and then read/write the register.</li> <li>3. Use digital I/O port. The way only access GPIO data register. Write data to this port will control the data output register. And read this port will read the pin status register.</li> </ol>

<Enter the Extended Function Mode>

WriteByte(AddrPort, 0x87)

WriteByte(AddrPort, 0x87)

// Must write twice to enter Extended mode

<Select Logic Device>

WriteByte(AddrPort, 0x07)

WriteByte(dataPort, 0x06)

// Select logic device 06h

WriteByte(AddrPort, 0x60)

// Select configuration register 60h (High Byte address)

WriteByte(DataPort, (0x0A))

```
WriteByte(AddrPort, 0x61)          // Select configuration register 61h (Low Byte address)  
WriteByte(DataPort, (0x00))
```

<Leave the Extended Function Mode>

```
WriteByte(AddrPort, 0xAA)
```

### 5.3.1.6 DATA Bit Table

GPIO-LED LED ON/OFF (GPIO00)

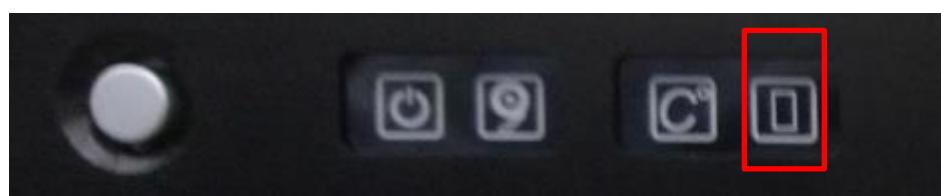
I/O Port data register address = Base address + 6 = 0xA06

7	6	5	4	3	2	1	0	bit
0	0	0	0	0	0	0	1	Value
1				/h				

= LED  
(Base address  
+6) (0xA06)

## 5.4 GPIO LED Status Definition

GPIO LED



LED Type	Status	LED Color
GPIO LED	GPIO activity	Green
	No activity	Off



# **Chapter 6**

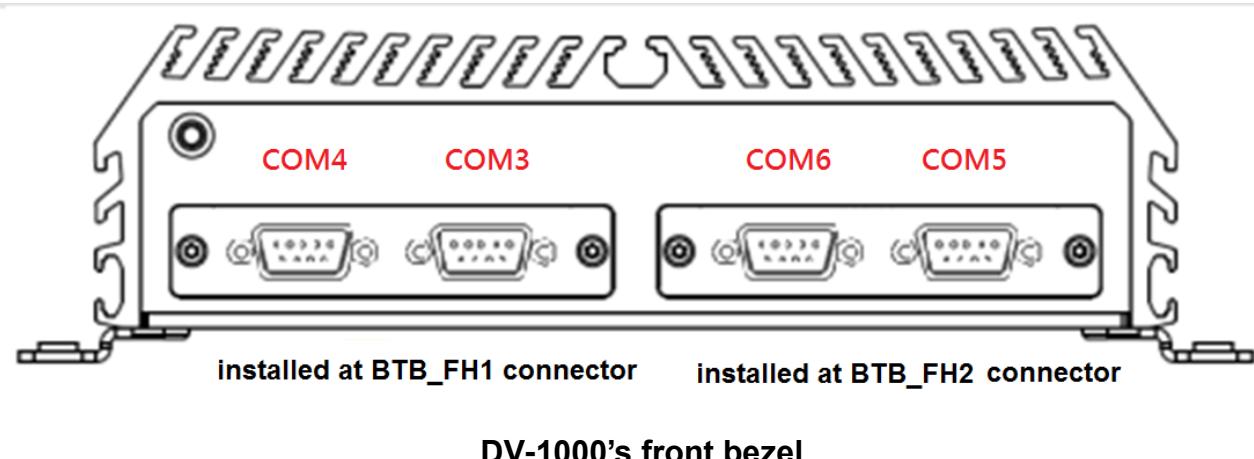
## **Optional Modules**

### **Pin Definitions and Settings**

## 6.1 Optional Module Pin Definition & Settings

### 6.1.1 CMI-COM06-R10/UB1603-R10 Module

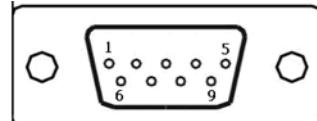
The CMI-COM06 module can be installed at BTB\_FH1 or BTB\_FH2 connector or both BTB\_FH1 and BTB\_FH2 connectors. If a CMI-COM06 module is installed at the BTB\_FH1 connector, the corresponding COM number is COM3 and COM4. If a CMI-COM06 module is installed at the BTB\_FH2 connector, the corresponding COM number is COM5 and COM6. If two CMI-COM06 modules are installed at both BTB\_FH1 & BTB\_FH2 connectors, the corresponding COM number is COM3~COM6 as shown below.



#### COM3~COM6: RS232 / RS422 / RS485 Connector

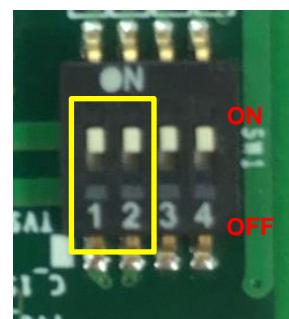
Connector Type: 9-pin D-Sub

Pin	RS232 Definition	RS422 / 485 Full Duplex Definition	RS485 Half Duplex Definition
1	DCD	TX-	DATA -
2	RXD	TX+	DATA +
3	TXD	RX+	
4	DTR	RX-	
5		GND	
6	DSR		
7	RTS		
8	CTS		
9	RI		

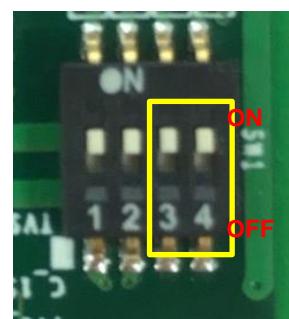


## SW1: COM3~6 Power Select

Location	Function		DIP1	DIP2
SW1 on CMI-COM Module	COM3/5	0V(RI)	ON (Default)	ON (Default)
		5V	ON	OFF
		12V	OFF	OFF



Location	Function		DIP3	DIP4
SW1 on CMI-COM Module	COM4/6	0V(RI)	ON (Default)	ON (Default)
		5V	ON	OFF
		12V	OFF	OFF

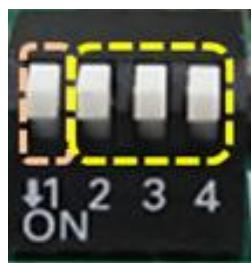


## 6.1.2 CFM-IGN04-R10 Module

### SW2 : IGN Module Timing Setting Switch

Set shutdown delay timer when ACC is turned off

Pin 1	Pin 2	Pin 3	Pin 4	Definition
ON (IGN Enabled) /	ON	ON	ON	0 second
	ON	ON	OFF	1 minute
	ON	OFF	ON	5 minutes
	ON	OFF	OFF	10 minutes
	OFF	ON	ON	30 minutes
	OFF	ON	OFF	1 hour
	OFF	OFF	ON	2 hours
	OFF	OFF	OFF	Reserved (0 second)



Default setting of Pin1 to Pin4 is OFF / OFF / OFF / OFF.

### 24V\_12V\_1: IGN Module Voltage Mode Setting Switch

12V / 24V Car Battery Switch

Pin	Definition
1-2	12V Car Battery Input
2-3	24V Car Battery Input (Default)



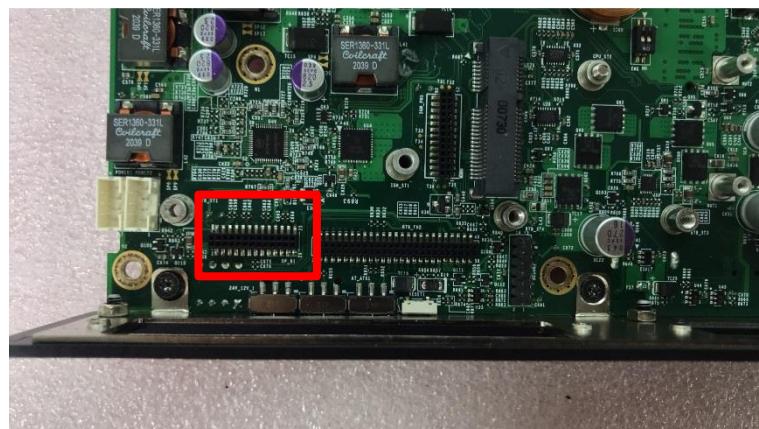
## 6.2 Installing High Speed CMI Module

### 6.2.1 CMI-DP01-R10/UB1606-R10 Module

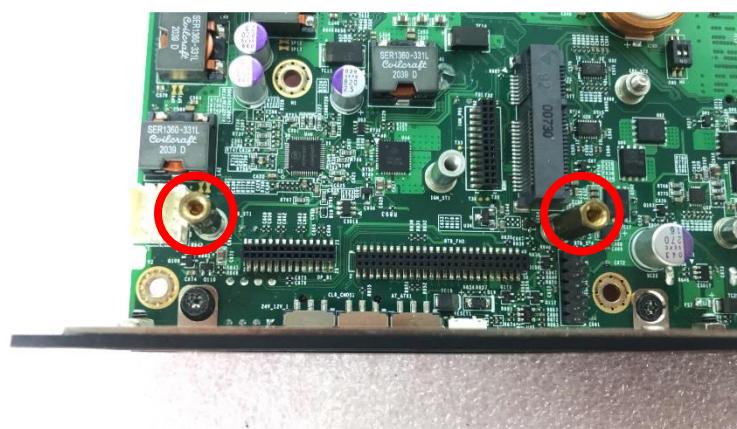
1. Unscrew the 2 screws to remove bracket from front panel.



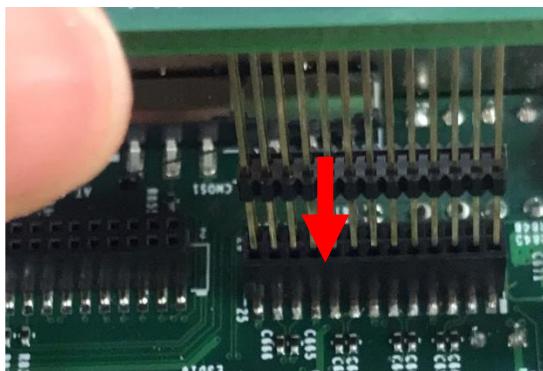
2. Locate the DP\_B1 connector.



3. Fasten the two copper pillar screws as indicated.



4. Insert the module vertically to the connector, and then fasten the 2 screws to fix it.



5. Attach on the CMI-DP01 bracket, and fasten the screws as indicated.

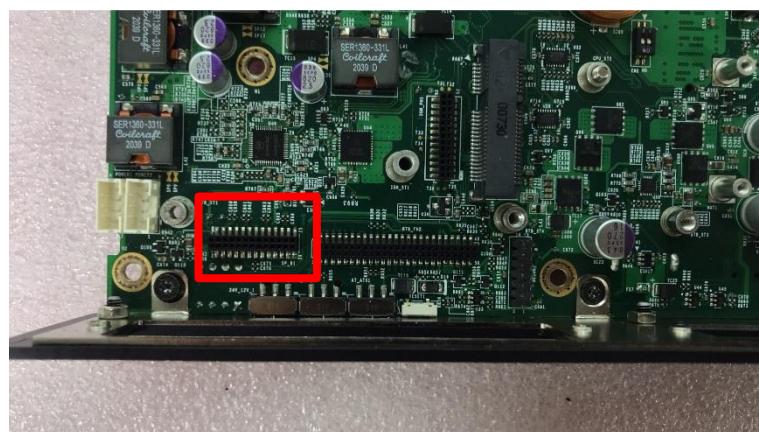


## 6.2.2 CMI-HD03-R10/UB1608-R10 Module

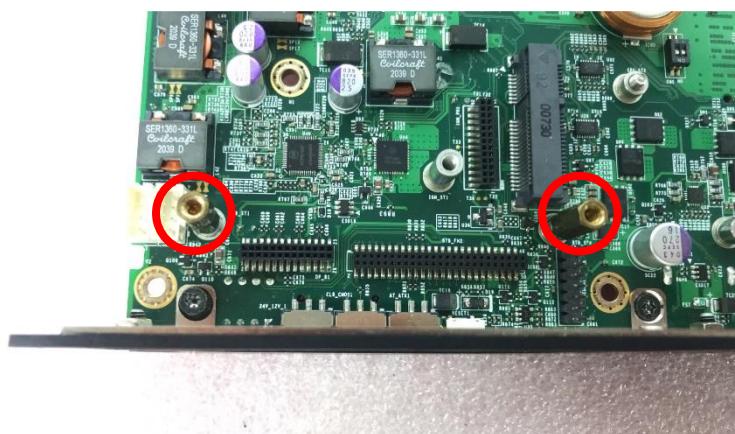
1. Unscrew the 2 screws to remove bracket from front panel.



2. Locate the DP\_B1 connector.



3. Fasten the two copper pillar screws as indicated.



4. Insert the module vertically to the connector, and then fasten the 2 screws to fix it.



5. Attach on the CMI-HD03 bracket, and fasten the screws as indicated.



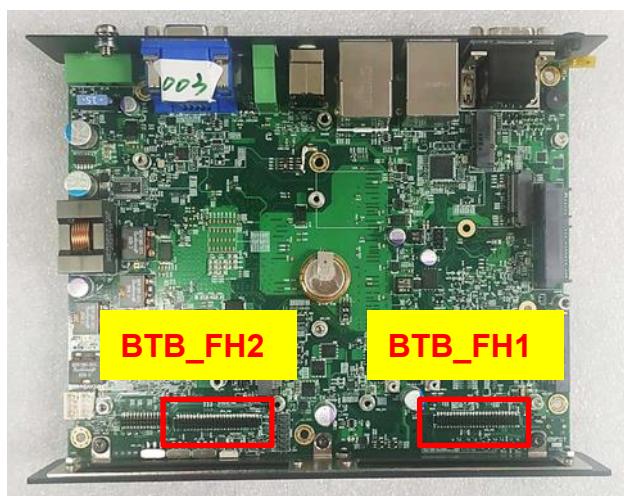
## 6.3 Installing Low Speed CMI Module

### 6.3.1 CMI-COM06-R10/UB1603-R10

1. Loosen the 2 screws on the bracket 1 or 2 at the front bezel and then remove the cover plate.



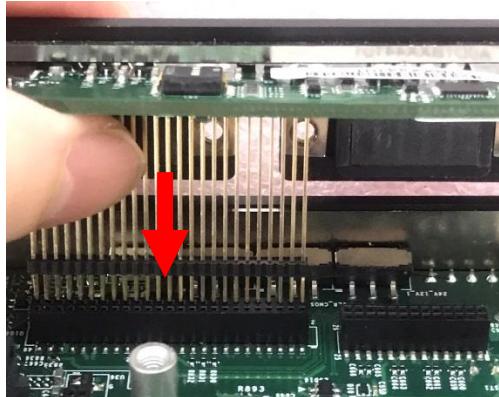
2. Locate the BTB\_FH1 or BTB\_FH2 connector.



3. Fasten the two copper pillar screws as indicated.



4. Insert the module vertically to the connector and fix it with the 2 screws.



5. Attach on the CMI-COM bracket. Fasten the 2 screws and 4 D-Sub jack screws to fix it.

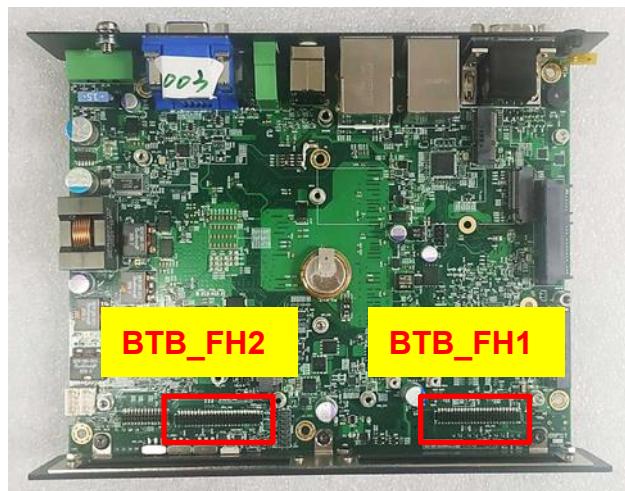


### 6.3.2 CMI-DIO06-R10/UB1618-R10

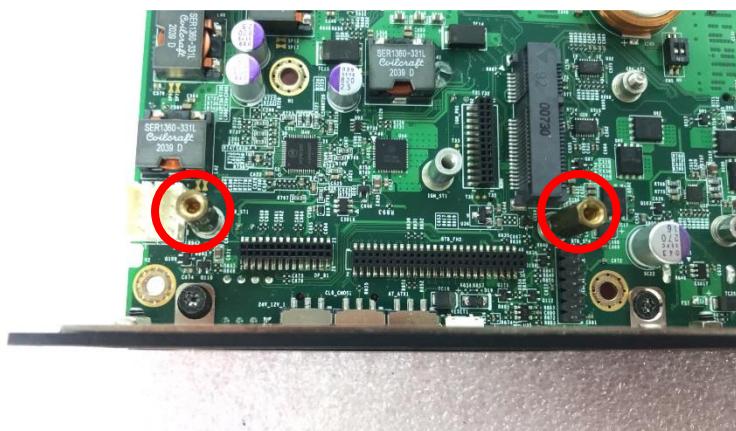
1. Loosen the 2 screws on the bracket 1 or 2 at the front bezel and then remove the cover plate.



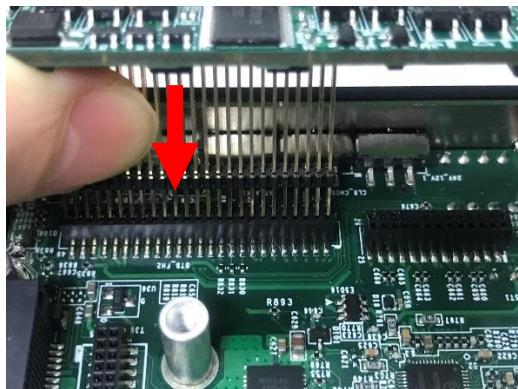
2. Locate the BTB\_FH1 or BTB\_FH2 connector.



3. Fasten the two copper pillar screws as indicated.



4. Insert the module vertically to the connector and fix it with the 2 screws.



5. Attach on the CMI-DIO bracket and fasten the 2 screws to fix it.



## 6.4 Installing CFM Module

### 6.4.1 CFM-IGN04-R10

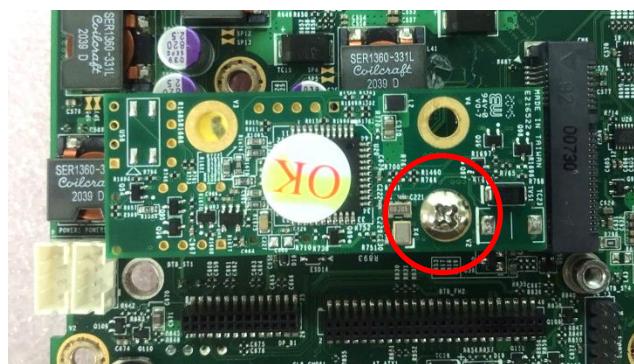
1. Locate the IGN\_PH1 connector.



2. Insert the module vertically to the connector



3. fasten the screw to fix it.



## 6.5 Installing MEC Module

### 6.5.1 MEC-USB-M102-15 /UB1614-R10

1. Loosen the 2 screws on the bracket 1 or 2 at the front bezel and then remove the cover plate.



2. Attach on the MEC-USB bracket, and fasten the 2 screws to fix it as indicated.



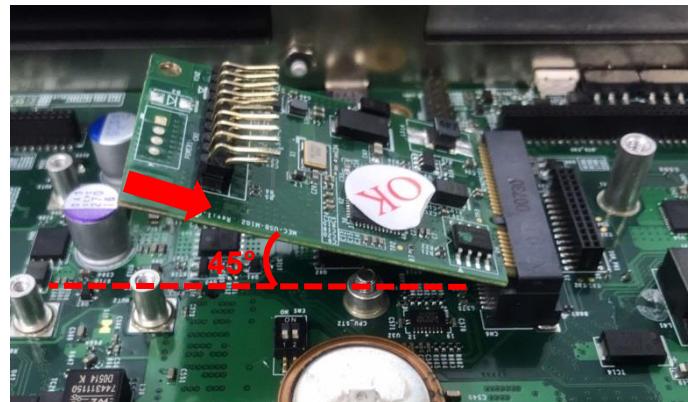
3. Locate the Mini PCIe socket(s) on the top side of the system.



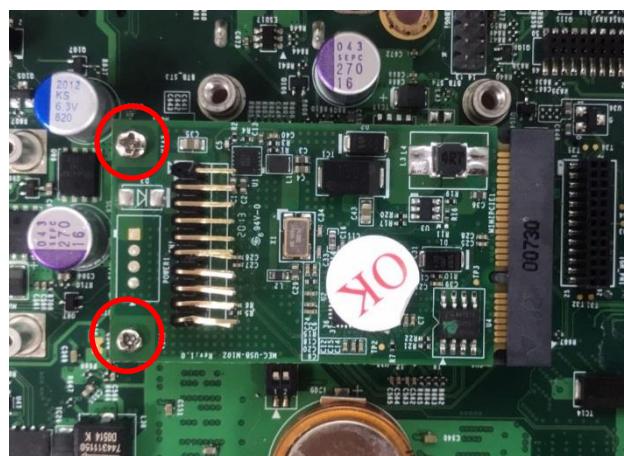
**NOTE**

MEC-USB module's mPCIe card can only be installed onto connector CN6, then the USB board can be installed at bracket 1 or 2.

4. Tilt the Mini PCIe card at a 45-degree angle and insert it to the socket until the golden finger connector of the card seated firmly.



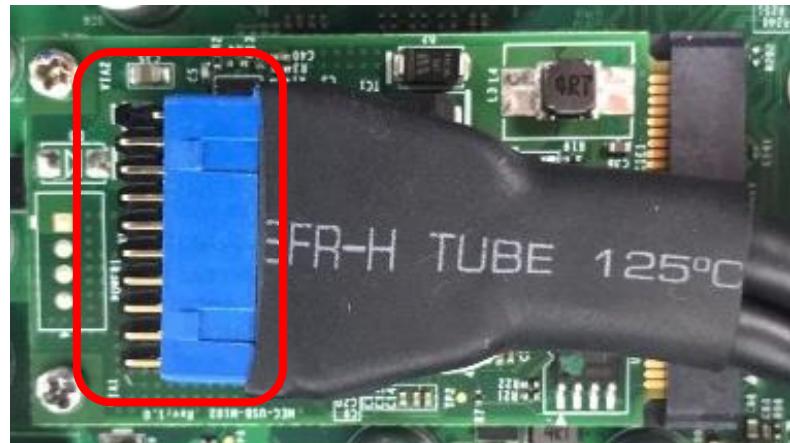
5. Press the card down and secure it with 2 screws.



6. Connect the attached wire to the USB board.



7. Connect the other end of the wire to the Mini PCIe card as indicated.



8. Attach the USB board onto the back side of the cover plate, and then fasten the two screws to secure the module.



## 6.5.2 MEC-LAN-M102-15/UB1611-R10

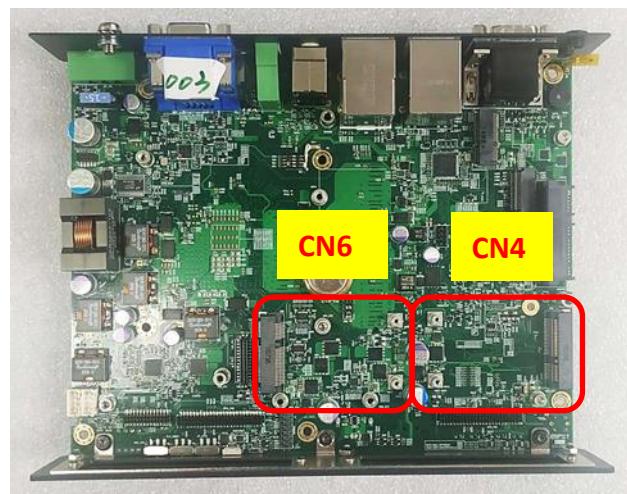
1. Loosen the 2 screws on the bracket 1 (left side) or bracket 2 (right side) and then remove it.



2. Attach the MEC-LAN bracket, and fasten the 2 screws to fix it as indicated.



3. Locate the Mini PCIe socket(s) on the bottom side of the system.



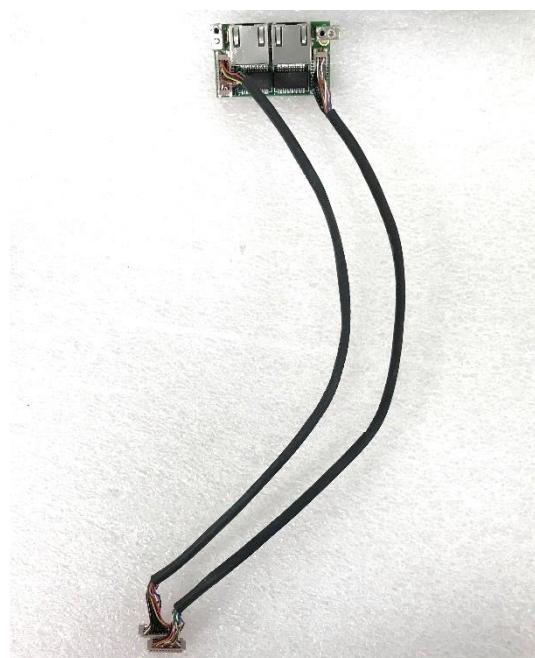
4. Tilt the Mini PCIe card at a 45-degree angle and insert it to the socket until the golden finger connector of the card seated firmly.



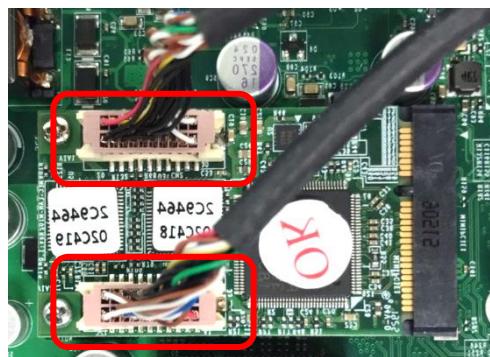
5. Press the card down and secure it with 2 screws.



6. Connect the attached wires to the LAN board.



7. Connect the wires to the Mini PCIe card as indicated.



8. Attach the LAN board onto the back side of the cover plate, and then fasten the two screws to secure the module.



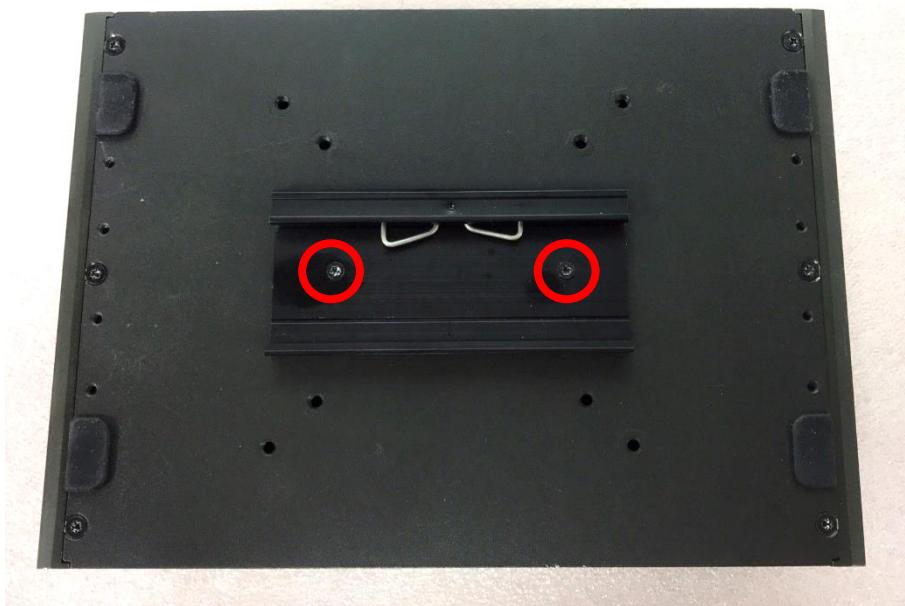
## 6.6 Installing Optional Accessories

### 6.6.1 DINRAIL-R10

1. Prepare the DIN-RAIL Mount Kit.

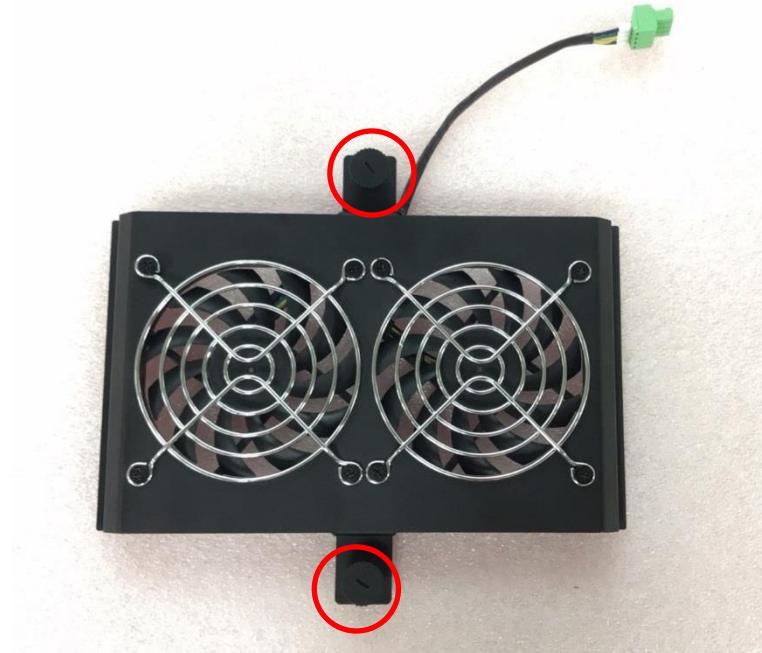


2. The mounting holes are at the bottom of system. Fasten the 2 screws to fix the DIN-Rail mount bracket with system together.



## 6.6.2 FAN-EX104

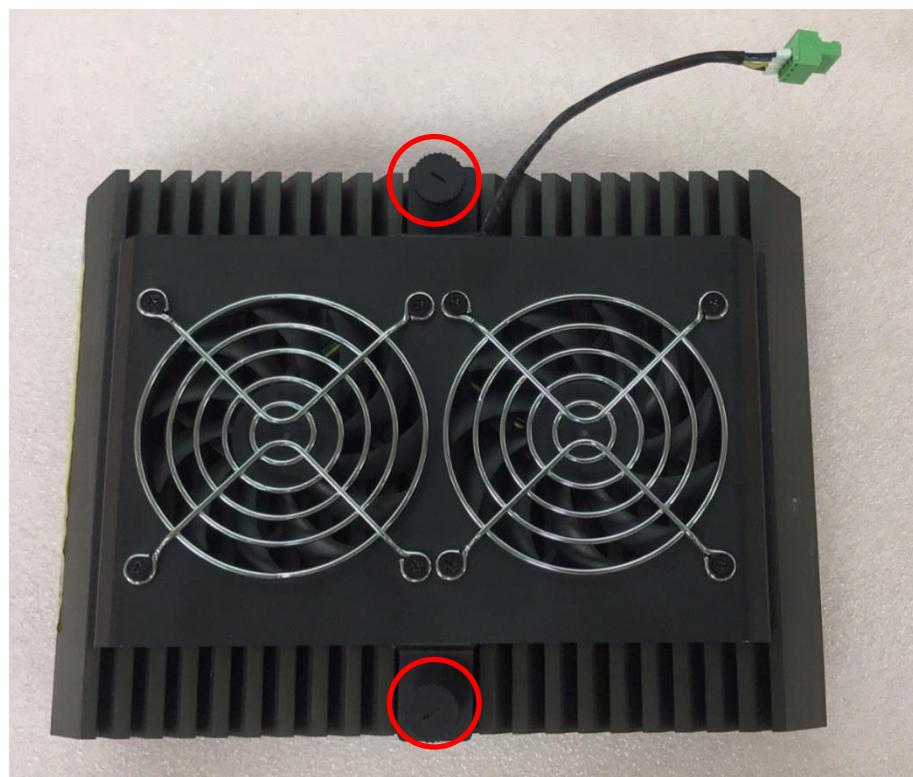
1. Prepare the external fan. Loosen the 2 screws halfway on mounting frame before attempting to install it.



2. Slide the FAN into the middle groove of chassis as illustrated. Tighten the 2 screws to fix it onto chassis.



3. Move the fan to the center of chassis. Tighten the 2 screws marked on photo to secure it.



4. Connect the FAN cable to external fan power connector at rear panel.



**cincoze**

© 2022 Cincoze Co., Ltd. All rights reserved.

The Cincoze logo is a registered trademark of Cincoze Co., Ltd.

All other logos appearing in this catalog are the intellectual property of the respective company, product, or organization associated with the logo.

All product specifications and information are subject to change without notice.